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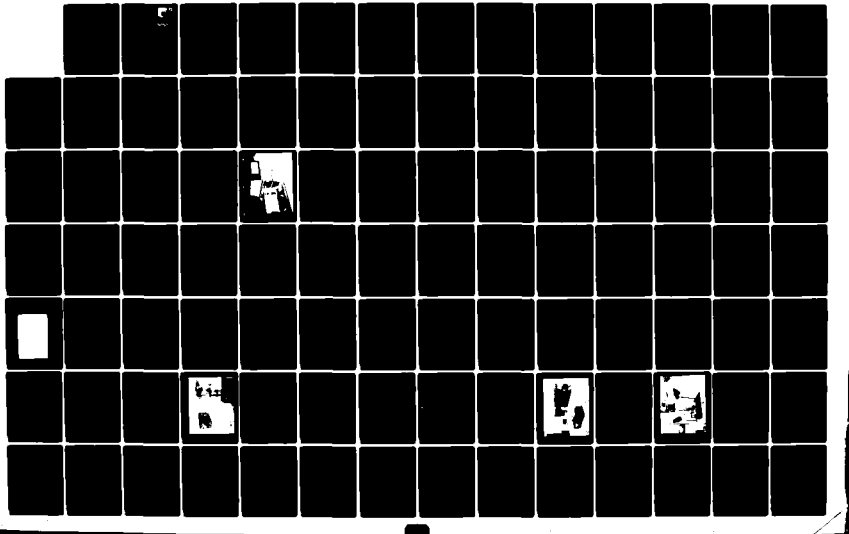

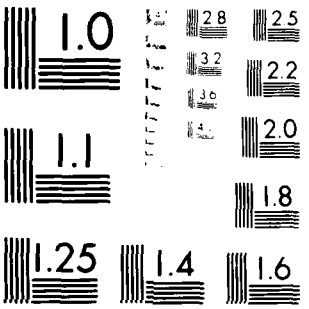

AFWAL-TR-83-3065

LED MULTIFUNCTION KEYBOARD ENGINEERING STUDY

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The Flight Dynamics Laboratory (USAF) and National Aeronautics and Space Administration (NASA-Langley) have jointly sponsored the LED Multifunction Keyboard Engineering Study. A programmable pushbutton switch (PPS) and an associated logic refresh and control unit (LRCU) were designed, fabricated and evaluated for their application in a multifunction keyboard (MFK). The switch employs an x-y dot matrix array of 11 x 35 green LED's to display up to two rows of six 5 x 7 characters. Graphic symbols compatible with the matrix array size may also be displayed. Up to four PPS units interface to - CONTINUED -

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data input sources through the LRCU via an RS-422 serial line. The PPS evaluation was conducted in two parts. In the first, the display parameters, mechanical and electrical characters of the PPS were assessed. Environmental and reliability testing was conducted. In the second portion of the study the effectiveness of the LRCU/PPS units as a part of the multifunction keyboard was assessed by operating the units with a multifunction controller designed for use with the switches. The controller availability permitted operation of the LRCU/PPS as part of a MFK system. All software commands and system operation aspects of the LRCU/PPS operated as designed. Areas requiring further design improvements include the use of more costly but efficient LED s to achieve sunlight readability, display luminance for sunlight readability, luminance step size and quantity, and display filter and moisture sealing.

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1.0 INTRODUCTION

This report describes the procedures followed and results obtained by Boeing and Micro Switch during the performance of Air Force Contract F33615-81-C-3624, "LED Multifunction Keyboard Engineering Study."

1.1 Purpose

The purpose of this report is to describe the background system definition which formed the basis for the study and to describe the procedures employed and results obtained in conducting the study. The study objectives were: 1) the evaluation of the performance of a sunlight readable multifunction switch using an x-y dot matrix LED array and incorporating tactile feedback and 2) definition and evaluation of a multifunction keyboard architecture to use the multifunction switch.

1.2 Scope

The procedures and results obtained in the course of this study were specifically directed toward the evaluation of the performance of a LED programmable pushbutton switch (PPS), developed by MicroSwitch, both as an individual unit and as a component of a multifunction keyboard (MFK). While the PPS display is limited to a single 16 x 35 LED array size, the procedures employed in the evaluation are applicable to LED switch displays in general. Similarly, the procedures and results obtained using the PPS units as a four switch MFK module are illustrative of the operation of larger keyboard matrices up to a maximum of 28 switches. The LED arrays were provided by Optotek, Ltd. of Canada.

1.3 Study Plan

The study is divided into three general areas of effort. First was the establishment of requirements for the switch function and MFK architecture and capabilities. The second covers the evaluation of the PPS switch/display module. Incorporated in this work are measurements of display parameters, electrical and mechanical characteristics, and environmental testing. The third area of effort involved the incorporation

of the PPS units and their associated logic and refresh control unit (LRCU) into a MFK system. Operation of the PPS within the MFK system was investigated with respect to MFK architecture, operator-MFK interactions, display luminance control, interface evaluation, display parameters, and system testing. A four switch data base was developed to perform the system tests. The original goal of the study was to modify a controller to accept four PPS units. A more versatile controller was developed in parallel with this study, however, and to improve the system test conditions, the new controller was used.

The study report is divided into six major sections. Section 2 describes some of the ambient conditions under which the switches would operate and some of the desired characteristics of the MFK system as a whole. Also included in Section 2 is a description of the MFK hardware and software architecture used in the tests. In Section 3, the measurements taken and tests conducted in evaluating the switch/display modules are described and the results presented. The MFK controller characteristics and the tests conducted with the switches operating as a MFK system are presented in Section 4. Section 5 describes conclusions resulting from the study. References are given in Section 6.

1.4 Summary

Tests were conducted on the PPS/LRCU units as individual modules and as part of an overall MFK system. The units produced legible displays in a format consisting of two rows of six characters. In addition, the capability for displaying graphic images was demonstrated. Optical measurements of display parameters indicate a low rate of defective pixels in the OPTOTEK displays, although the variance of pixels from the mean is larger than the goals set forth for the study. The display luminance is sufficient to provide a contrast ratio of 3 at an ambient light level of 10,000 fc for monolithic LED displays, but not for discrete LED displays. Measurements were conducted on both monolithic and discrete arrays of LED's. The contrast ratio was higher by a factor of approximately 2.5 for the monolithic displays although the cost is higher and the availability of these displays is more limited. Crosstalk in the displays was not a problem with the exception of the lowest luminance level where electrical crosstalk between rows was caused by the drive electronics timing. The viewing angle

measurements of the displays showed adequate relative contrast ratio within a 45^{o} viewing angle cone.

The PPS/LRCU units were tested as part of a MFK system programmed to exercise the LRCU display and luminance control commands. In the development of the testing procedure, evaluations of the architecture of a MFK system were conducted. An RS-422 serial interface was selected to interface each group of 4 PPS units with their associated LRCU to the processor forming the MFK controller. The host to MFK controller interface was handled by an RS-232 interface. The controller software provided to operate the PPS/LRCU units enabled all the commands and operating modes of the units to be tested. Tests included luminance control, power levels, response time, legend and command storage, data base logic tree storage, uploading and downloading of information between the controller and the host, and verification of command transfer and proper legend display. Automatic and manual luminance control capability were demonstrated successfully although the automatic sensor requires an increased dynamic range. On the PPS/LRCU units the luminance steps require greater resolution at lower levels to avoid a noticeably discrete transition between luminance steps. Power levels were measured at approximately 1.3 watts/switch including the share of the LRCU associated with that switch. This figure is within the study requirements but somewhat higher than the desired goal.

A data base designed to operate with four PPS switches was coded into the MFK controller and used to test system functions of a MFK. Legend and command storage, data and command transfer and correct logic tree response of the system was verified. The response time for keyboard legend update was measured and found to meet the study goals of less than 0.2 seconds.

As a whole the PPS/LRCU units operated quite successfully considering their development status. The study provided an excellent opportunity to identify those areas needing further development effort.

2.0 SYSTEM DEFINITION

An essential step in the formulation of tasks to be done in the study was the development of a set of requirements for the capabilities of an MFK as well as for the PPS/LRCU modules which are to make up the keyboard. Many of the requirements, particularly those for the PPS/LRCU were taken from Air Force E/O Keyboard Request for Proposal (Reference 2-1). Others were developed in the course of the study and by parallel work being carried on at Boeing.

Potential applications of a MFK system were surveyed for both tactical and commercial aircraft. In the commercial sector, personnel at Boeing, NASA-Ames, NASA-JSC and Eaton were contacted for information on potential uses of MFK systems. The system was described to them and their comments were invited on possible uses. At Boeing, the MFK system is also under development in the commercial division. Applications considered include checklist handling, flight management, electrical system control and environmental system control. The commercial advanced cockpit design group is currently looking at preliminary applications of the PPS for the Terminal Controlled Aircraft (TCV) program at NASA-Langley. NASA-Ames personnel were interested in the PPS switches for use in a flight management. NASA-JSC was interested in the use of the MFK system as a general control device for Orbiter systems. Candidate systems for control include the electrical, orbital maneuvering, environmental, guidance and navigation and reaction control system. Eaton was primarily interested in the MFK concept for the centralized control of aircraft electrical circuit breakers and loads. In summary, major use of MFK systems in commercial aircraft lies in the handling of checklists and preflight or prelanding procedures. With the advent of increasingly computerized flight systems, the capability of a MFK system to handle those functions automatically, semi-automatically or manually (at crew option) is greatly increased. Another area of application of a MFK in the commercial sector is in flight management activities where several different modes of operation are needed occasionally during different portions of the flight.

Tactical aircraft applications of MFK systems have been described in the study by Graham (Reference 2-2). These include navigation, weapons delivery, stores management and communication. An important consideration in tactical aircraft is

the minimization of operator workload in high threat or weapon delivery situations. These points were brought out in discussions with naval aviation personnel and with a Boeing group involved in development of advanced avionics concepts for tactical aircraft.

In defining the MFK architecture and hardware, it was found that the design of the MFK system itself was quite similar for either commercial or tactical aircraft. The data base for the particular application and the initial conditions for the system, such as number of switches would form the only major differences. Thus the various aspects of the study were not considered separately for the two types of aircraft.

2.1 Required Functional Features

A number of basic features were required for the PPS/LRCU modules and for the MFK system as a result of the initial definition of the study. These features are described in the following subsections.

2.1.1 Programmable Legends

The PPS modules were to consist of 16 X 35 LED dot matrix arrays with a resolution of 40 lines/inch. The objective was to provide a fully programmable array capable of displaying characters in a number of font sizes or styles as well as graphic symbols fitting within the limits of the matrix. This choice of resolution and matrix size provided a maximum number of two rows of six 5 X 7 ASCII (Reference 2-3) characters.

2.1.2 Tactile Feel

The PPS modules were to incorporate a mechanism for providing a positive tactile feel to the operator when the switch was activated. As yet, the optimum force curve required for activation has not been determined due to changing requirements for protective clothing which might be worn by the crew.

2.1.3 Modularity

The MFK system was to be constructed from modular components to permit flexibility in locating the system within an aircraft cockpit. The general layout of an MFK system together with a desirable configuration of modular divisions is shown in Figure 2.1.3-1. The physical division of modular components is indicated by the dashed boxes. This division permits location of the controller and power supplies in a remote location from the PPS units thus offering the option of conserving panel space. The heavy solid lines indicate the physical division of components to be used in a 20 switch MFK being developed as a demonstration unit at Boeing. The LRCU's and PPS units are contained in the block labled "20 SWITCHES". The lower block surrounded by a heavy solid line inciudes the components in the keyboard portion of the unit. The upper solid line block contains the components of the controller portion of the unit. The internal configuration of the controller will be shown in greater detail later in the report. The modularity of the PPS units will allow the "keyboard" to be distributed in a large number of possible panel configurations (including multiple small keyboards, if desired). This feature is particularly important in considerations of retrofitting existing aircraft with MFK hardware.

2.1.4 Host-MFK Interface

One of the principal reasons for the development of an MFK system is the ability to include sufficient intelligence within the MFK to offload the display processing, legend storage and logical structure of the system from the aircraft host computer. In this study the goal was to develop an interface architecture which minimized the necessary transfer of information between the MFK and the host computer within the constraints of system reliability. For the purposes of this study, the physical link between host and MFK controller was defined as an RS-232 serial line.

2.1.5 Optional Data Bases

One of the current difficulties with command, control and communication (C^3) systems is the inability to easily adapt the system to the inclusion of new hardware or mission constraints. The MFK concept is designed to reduce this difficulty by operating with a flexible software data base which is pertinent to a particular set of

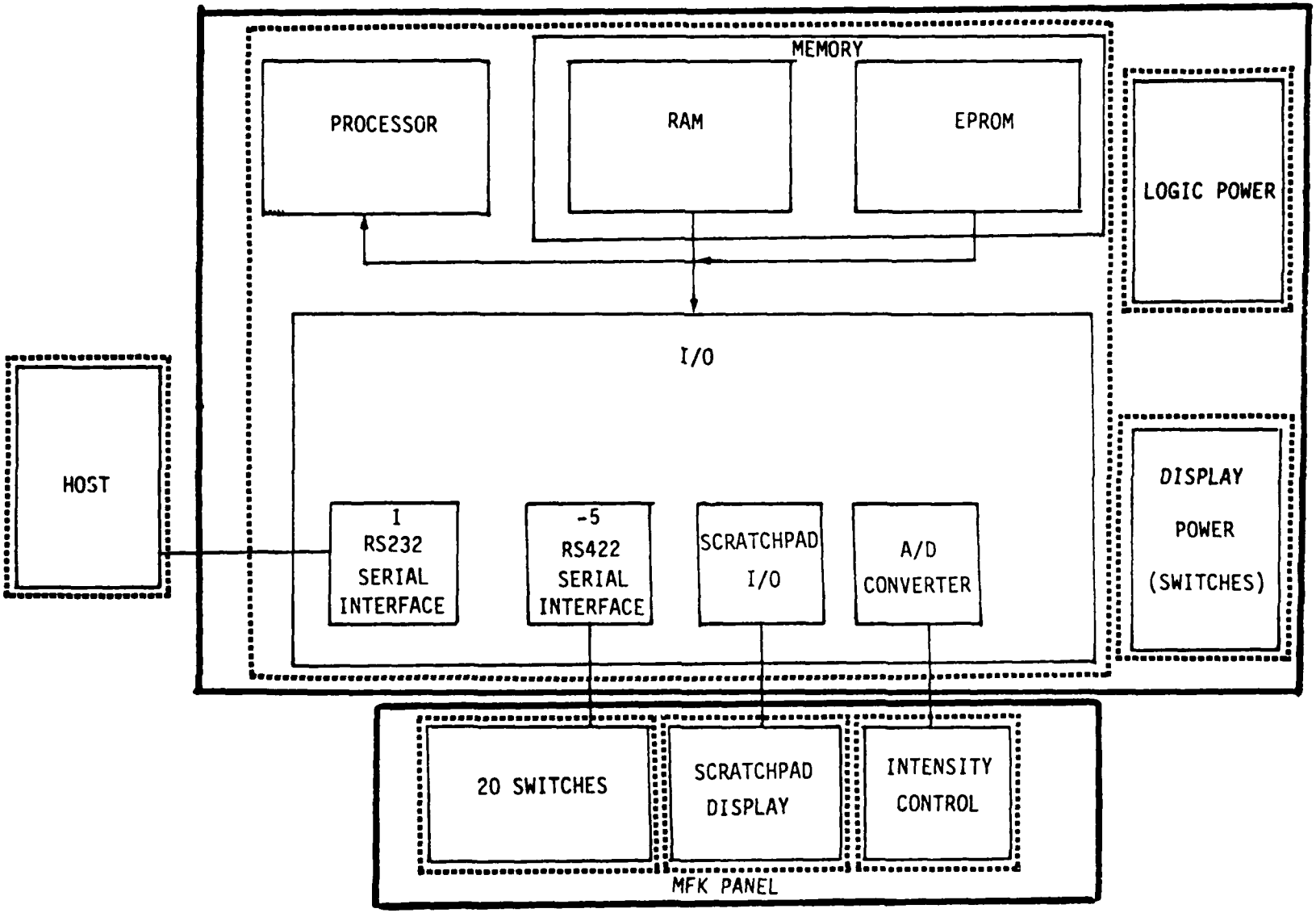


Figure 2.1.3-1: MFK BLOCK DIAGRAM

hardware and/or mission requirements. If the hardware or mission requirements change then the MFK would need only a reconfiguration of the software data base to a form compatible with the new hardware or mission requirements. For multiple mission aircraft the host computer could store a number of data bases and operate with any one in the MFK by downloading the appropriate data base from the host to the MFK controller. Thus the capability for downloading information from the host to the controller is an important part of the MFK design.

2.1.6 Multiple Configuration Capability

An MFK system as initially considered in the study included of a keyboard of PPS modules with the addition of a small (2-3 line, 24 character) scratchpad area for data entry and host MFK messages. In the course of the study, consideration of parallel work indicated that a general MFK system might well include larger scratchpad areas and/or higher resolution displays. Some possible options for the MFK configuration are shown in Figure 2.1.6-1. These options were developed as part of a NASA study on the application of multifunction displays and controls to the Orbiter (Reference 2-4). As a result of these considerations a goal was adopted of including within the general MFK architecture the option of adding these additional displays in a modular fashion. Several means of doing this were considered in the overall MFK architecture design.

2.2 Human Factor Requirements

A number of the features of an MFK system depend on the particular application and environment for which it is intended. These features typically include human factors considerations to provide a suitable interface between the operator and the system.

2.2.1 Display Parameters

The format of the PPS displays was defined as part of the initial conditions of the study. The 16 x 35 green LED matrices were supplied by OPTOTEK of Canada for incorporation into the Micro Switch PPS units. One of the study goals was to evaluate the display performance in terms of brightness, uniformity, color and contrast ratio as a function of viewing angle. The ambient light range of interest was taken as 10^{-6} to 10^{4} fc, corresponding to light level ranges anticipated in tactical aircraft cockpits.

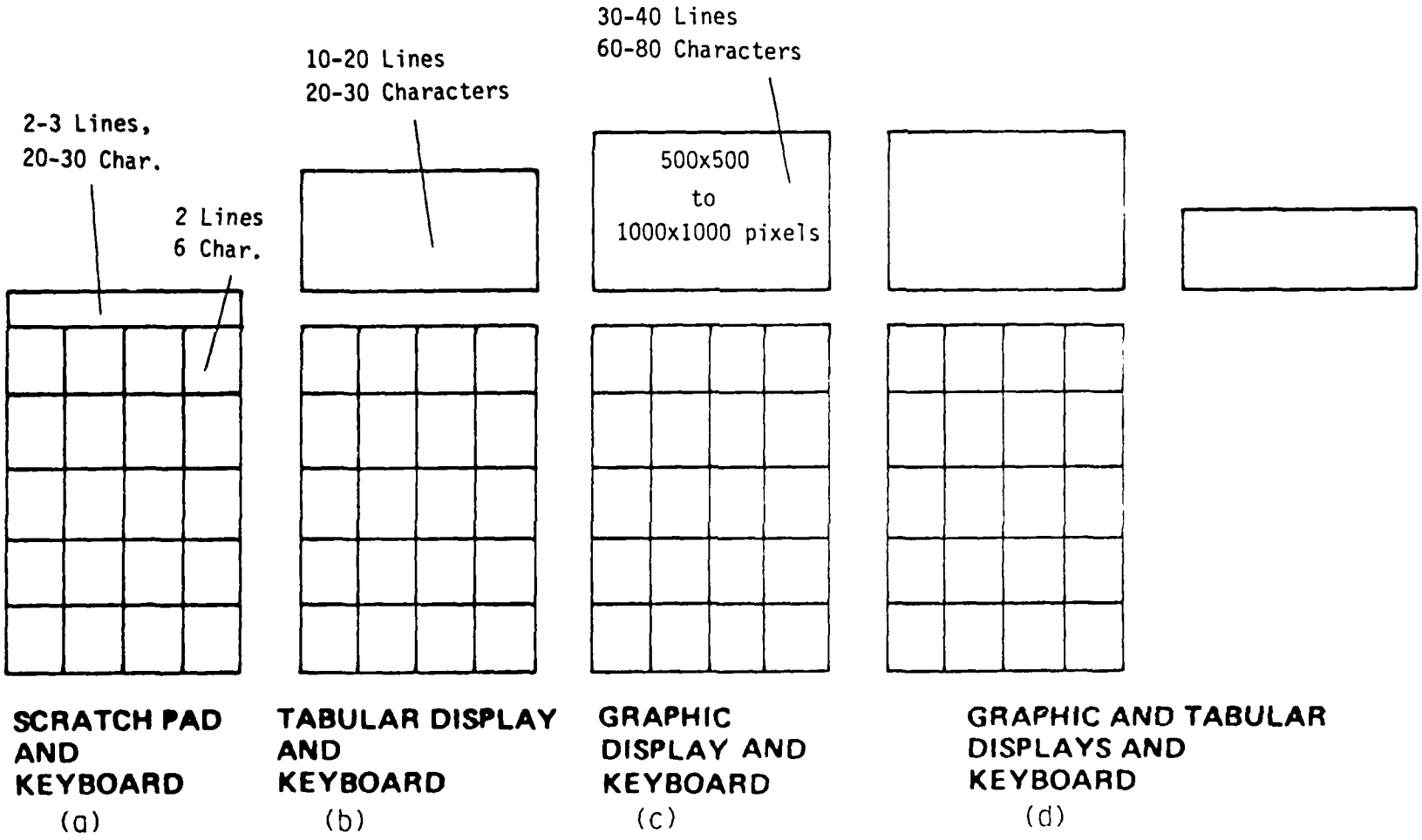


Figure 2.1.6-1: MFK Display Options

2.2.2 Character Parameters

The choice of character size, spacing and font style for alphanumeric characters has been studied at some length, particularly for CRT displays. For dot matrix flat panel displays, a primary difference is the sharp edges of the emissive areas relative to the blurred edges of a CRT pixel. Several recent studies have been conducted on font styles and matrix displays (References 2-5, 2-6). For the matrix format chosen, the principal font is limited to 5 X 7 dot characters if the desired two rows of 6 characters are to be displayed. Similarly, the intercharacter spacing is limited to one column of LED's.

2.2.3 Indenture Levels

The typical MFK system replaces a larger number of dedicated switches with programmable legend switches. As a result the functions of the individual switches are often reached through a logical tree of individual switch actions. A typical sequence is shown in Figure 2.2.3-1. The maximum number of switch actions to reach a particular function (i.e., the maximum number of levels of indenture) should in general be kept at a minimum if the workload is to be improved by use of the MFK system. The time to access a particular function increases with the number of operator actions required (Reference 2-7). In interviewing a military test pilot on the number of indenture levels, it was found that indenture levels greater than four, after the initial page, were felt to be cumbersome. More importantly, a need for automation of procedures was found to exist where procedures required repeated cycling back to the top level. The application to tactical aircraft would, in general, require a lower number of indenture levels because of the tighter time requirements, number of threats and terrain proximity relative to commercial aircraft operation.

2.2.4 Access Schema

In an access schema for a MFK system there are a high number of possible ways of reaching a particular switch function. A choice must be made between a large number of switches in the keyboard and minimal indenture levels and a small number of switches and more levels of indenture. Care must be taken to ensure that the operator can always return to the top level of the logic tree when desired and that no switch action or switch failure results in a lock-up of the MFK system function.

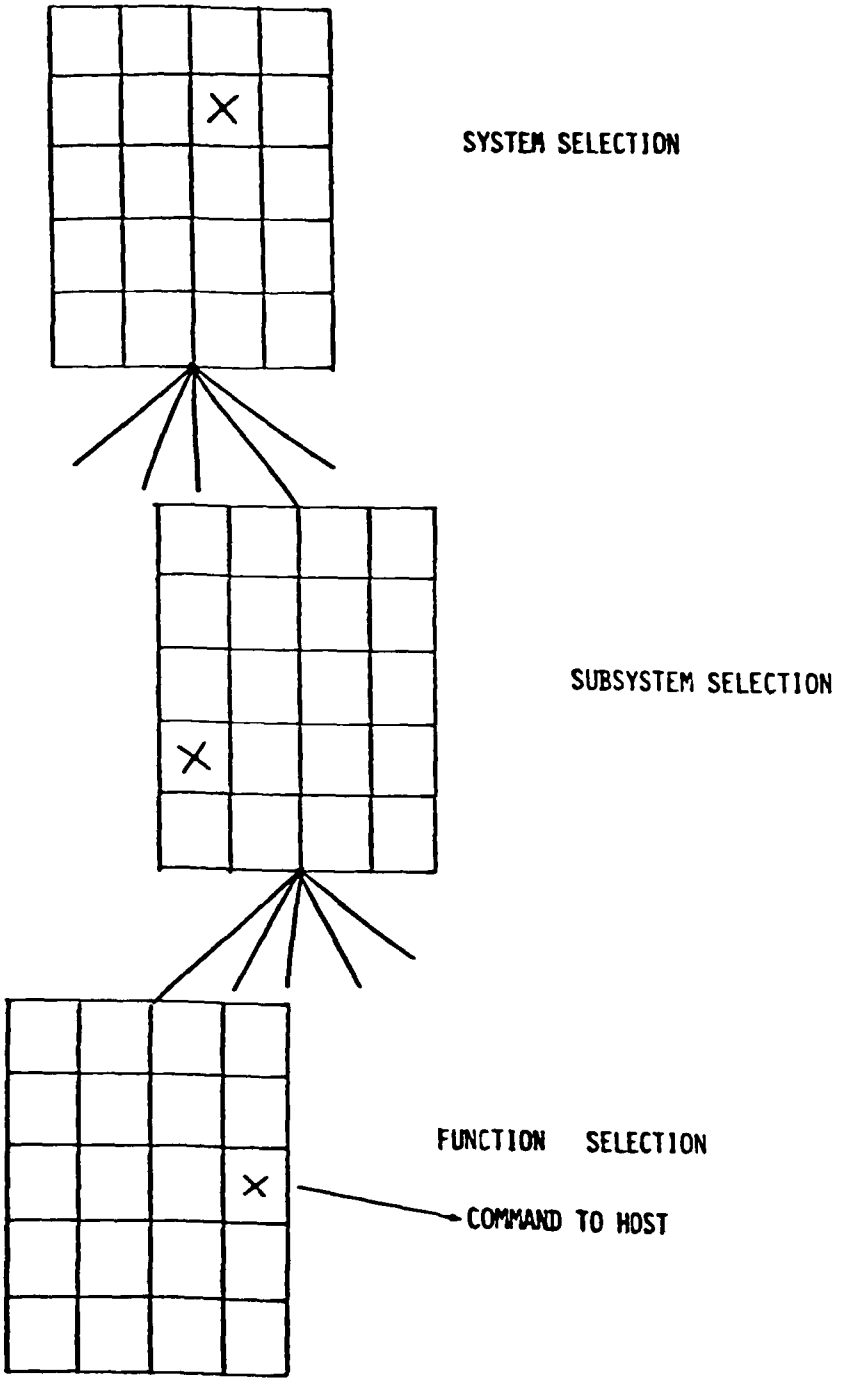


Figure 2.2.3-1: MFK SWITCH ACTION SEQUENCE

Thus, a means for working around individual switch failures should be provided. In a typical system, some switches will be used so frequently, or are so crucial when needed that the functions they control require a dedicated switch. A large part of the access schema design for an MFK consists of evaluating all the functions considered for inclusion in the logic tree and deciding which to retain as dedicated switch functions and what the relative levels of subordinance are for those remaining.

2.2.5 Operator Cueing

Another important MFK capability is the option of alerting the operator to certain conditions (i.e., caution and warning) by forcing a particular display feature on the MFK switches or scratchpad. This cueing of the operator may be done in various ways using the PPS's themselves. One method is to force one switch to a blinking state. By pressing the blinking switch and a following series of blinking switches, the operator can be led through a particular procedure or to a function which requires his attention. Alternatively, a particular display can be forced onto the keyboard by a message from the host computer.

2.2.6 Luminance Characteristics

Basic goals for the evaluation of the PPS modules with respect to luminance were taken from the requirements of Reference 2-1. The following definitions were used in the description of the evaluations and tests conducted:

1. Display Image Luminance (L_S) - The spatial average of luminance readings taken within the character area.

2. Display Background Luminance (L_D) - The luminance in the area of the display immediately surrounding the "on" character image is termed the "on" display background luminance and is designated L_{DB}. The luminance of the pixel with the character image turned "off" is termed the "off" display background luminance and is designated L_{DS}.

3. Perceived Luminance (ΔL_P) - The luminance that is visually perceived is the difference in luminance between the "on" and "off" pixel element and is defined by the equation.

$$\Delta L_P = L_S - L_{DS}$$

4. Image Contrast Ratio (CR) - The ratio of perceived luminance, ΔL_P, to the off display background luminance L_{DS} is defined as the display image contrast ratio, CR, where

$$CR = \frac{\Delta L_P}{\overline{L_{DS}}}$$

Contrast Ratio - To provide adequate display legibility, a contrast ratio goal of CR 3.0 was assumed for viewing normal to the display surface. This CR was to be maintained up to an ambient light level of 10,000 foot-candles (fc) of either diffuse surround illumination, direct incident-sun illumination or any prorated combination of sun and sky illumination.

Image Luminance Control - The desired operating range of ambient illumination was taken to be 10^{-6} - 10^{4} fc. Considerable image luminance control is required for legibility and viewing comfort over this range.

Figure 3.1.1-5 (page 64) gives the perceived luminance control requirements ΔL_P for reflected display background luminance values, L_{DS}, in the range from 10^{-6} foot-Lamberts (fL) to 10^{+4} fL. The lower bound of the required luminance control region represents an approximately constant comfort level of legibility as the reflected luminance varies in response to exposure of the display to illuminance levels from 10^{-6} to 10^{+4} ft. Minimum luminance requirements corresponding to normal, $\theta=0^{\circ}$, and 45° off axis viewing angles are shown. Within the required luminance control region, curves of approximately equal legibility satisfy the control law

$$\Delta L_P (L_{DS}) = \Delta L_{pc} + (1.42 + 49\ \Delta L_{pc})\ L_{DS}^{0.926} \quad fL$$

where increasing L_{pc} values in the range (i.e. see ordinate axis of Figure 3.1.1-5):

$$0.05\ fL < L_{pc} < 2\ fL$$

produce increasingly higher levels of viewing comfort.

These requirements and Figure 3.1.1-5 are taken from Reference 2-1.

Viewing Angle - Viewing angle requirement goals were also derived from the relation shown in Figure 3.1.1-5. For individual pixels, a 45^{o} cone viewing angle is desired while the switch bezel structure, filtering and display arrangement on the keyboard should permit an unobstructed viewing angle cone of 30^{o} measured from the normal to the keyboard center.

Veiling Luminance - Veiling luminance caused by high surrounding light levels in the operator field of view can cause a higher requirement for perceived display luminance. Part of the display evaluation requires the evaluation of this factor.

Crosstalk - An undesirable feature of the display operation is crosstalk which may be induced optically or electrically. Optical crosstalk can be caused by interdiode transmission and reflections causing apparent emission from non-excited diodes. Electrical crosstalk can result from low diode excitation thresholds or connection problems in the display. Basic requirements assumed for crosstalk were:

1. Optical crosstalk - $\Delta L_{oc} = L_{DB} - L_{DS} < 0.05\ \Delta L_{P}$
2. Electrical crosstalk - $\Delta L_{ec} < 0.02\ \Delta L_{P}$

Luminance Uniformity

The requirements of Reference 2-1 were taken as the basic goals for luminance uniformity with respect to intensity, color and perceived flicker. The pixel uniformity goal is a limit of $\pm$25% maximum variation from the mean luminance/pixel for a display matrix. The allowed average luminance variation from matrix to matrix was taken as 10% for matrices forming a keyboard. The background luminance variation for both pixels and displays should be less than 15% of the average background luminance. The assumption was also made that flickering would not be acceptable and that longer term temporal variations (drifts) due to loading or environmental conditions should be kept below 5%. Display image color is, in effect, fixed by the choice of the green Optotek LED arrays as the display medium.

Fingerprint Effects

The deposits left by fingerprints can effect reflections and transmissions in optical components. Part of the study plan includes the assessment of the effectiveness of various means of reducing the effect of fingerprints on the switch/display module performance.

2.3 Hardware/Software Requirements

The following subsections describe some of the requirements for hardware and software imposed by the features needed in a MFK system and the environment in which the system should operate.

2.3.1 Legend Display Capability

The ability to display programmable legends on the switch/display modules requires that the software and hardware on the PPS/LRCU sets be designed to accept full matrix display inputs as well as ASCII characters. Part of the original design of the Micro Switch PPS/LRCU modules called for this feature. Part of the study plan included the evaluation of this capability using the MFK controller.

2.3.2 Reaction Time

Reaction time requirements for a MFK system should be based on operator requirements for system response to a switch activation. A goal of < 0.2 second was assumed for the maximum reaction time needed for updating the legends on the keyboard. A somewhat higher goal of < 0.8 seconds was set for the scratchpad display. These goals were derived from Reference 2-1 and from human factors estimates made at Boeing. These goals were used as guidelines for choices on the MFK architecture discussed in Section 4.

2.3.3 Power

A basic problem with LED displays is a high level of power consumption. The displays used in the PPS units were chosen in part because of their high efficiency. In addition

to overall power consumption, the low efficiency of the LED's presents potential heating problems for the PPS unit itself, the keyboard assembly and the operator. Maintenance of the activation surface of the switch at $<115^{o}F$ was desired for steady state operation. Initial estimates thus indicated a maximum allowable power dissipation of 2 watts/PPS module including the LRCU power. A power dissipation of one watt/PPS module was taken as a goal for this study.

2.3.4 Switch Activation

Several features are required as part of the switch activation mechanism for the PPS units. Contact debouncing circuitry is preferrable to performing this function as part of the software processing. This feature is provided by the use of the Hall effect switch in the PPS module. Activation of the switch by pushing on the display surface requires a moveable display filter and sufficient ruggedness to provide reliability and protection for the display. The need for tactile feedback requires the incorporation of a suitable feedback mechanism in the switch structure.

2.3.5 Switch Location

One of the requirements imposed by modularity of the PPS units and the optional choice of PPS location is a need for hardware and software capable of driving the lines to remote switches. The architecture between the PPS/LRCU and the MFK controller is thus limited by the requirement for possible remote switch locations. Similarly, the physical structure of the PPS/LRCU modules is constrained by this requirement. Ideally, the components of the LRCU would be incorporated in each PPS module. At this stage of development, however, the definition of the unit requirements is not complete enough to proceed to that stage in a short time period. As a result, the four switch LRCU module has been employed as the interface between the PPS units and the MFK controller.

2.3.6 Legend and Command Storage

The capacity for storage of legends and commands is primarily a function of the MFK controller memory capacity. A limited legend storage capability can be included in the LRCU depending on the choice of architecture for the MFK software. As part of

the study, estimates were made of memory requirements for storage of legend pages and of the probable number of pages required.

2.4 Environmental Constraints

The PPS units, as currently developed, will not satisfy the requirements for militarily qualified hardware for tactical aircraft use. A goal of this study is to determine their performance over the range of environmental parameters for which they were designed and to use this information as a base for further improvements.

2.4.1 Temperature

Temperatures encountered in tactical aircraft can be as high as 95°C for short time periods. For example, specifications for an LED display in the F-16 require operation at 95°C for 2 minutes after turn-on. In addition, the cooling for much of the F-16 flight panel instrumentation relies on ambient air convection for cooling. Tests were conducted over an operating temperature range of -40° to +55°C for the PPS units and -40° to +65°C for a nonoperating condition. At this stage of development not all the integrated circuits are rated for 95°C temperatures although a development objective is to increase the temperature operating range.

2.4.2 Vibration and Shock

The PPS/LRCU units are designed for eventual use under conditions found in both jet and turboprop aircraft. The vibration and shock testing therefore follows the accepted military standard procedures for testing electronic components. The major concession made to the development status of the units was the removal of the heat sink on some samples during vibration and shock testing. This component of the assembly could currently require support in an aircraft installation.

2.4.3 Altitude

The PPS/LRCU units are planned for use in all phases of aircraft operation including unpressurized high altitude flight and rapid changes in altitude. As a result testing of the units was required over the full range of altitude and altitude change rates

required for military qualification. Since the units are not completely sealed, the possibility of corona or other electrical discharge must be considered. Although operating voltage is low for these devices the combination of low atmospheric pressure and high field strengths at sharp projections within the circuitry should not be ruled out as a possible problem source.

2.4.4 Humidity

Humidity will vary from near 0 to 100% in projected environments for the PPS/LRCU units. The development units were not specifically constructed to withstand high humidity or moisture levels. Humidity tests were conducted in accordance with military specification requirements to establish areas of the switch module requiring further development or protection for high humidity operations. Currently, moisture seals have been included in the activation surface of the switch and methods of sealing the electronics are being investigated by Micro Switch.

2.5 Specification Document

The PPS/LRCU units currently produced are basically one stage in a continuing development of the PPS. As part of the development process, the specifications thought to be appropriate for the PPS/LRCU unit have been written up in the form of a specification document. (Reference 2-8.) This document describes the requirements for design and construction of PPS and LRCU units, the hardware and software interfacing, modes of operation and provisions for growth in the PPS display capabilities. The document is intended as a guideline for future improvements in the switch and lists numerous conditions not met by the current model. In general, the specification document aims toward a fully militarily qualified PPS/LRCU unit. The document has undergone several revisions in draft form which consist primarily of updates to the desired features of the PPS/LRCU units as their development progresses.

2.6 Multifunction Keyboard System Description

The following subsections provide a description of the MFK system configuration used in the tests conducted during the study.

2.6.1 MFK Controller

The original study plan called for the modification of an existing Boeing controller to drive a set of four multifunction switches. As the study began, a parallel Boeing effort was started to develop a demonstration MFK using the Micro Switch PPS's and LRCU's. As a result, the new controller was actually used in the study since its architecture was tailored to the PPS/LRCU units and provided a better evaluation of the capabilities of the PPS and associated LRCU.

The controller was developed using readily available comercial components to minimize design time and associated costs and to permit configuration flexibility. The general layout of the MFK development system is shown in Figure 2.6.1-1. The controller is based on an Intel Multibus structure and uses an Intel 80/30 single board computer as the controller processor (8085 microprocessor). The memory installed on the 80/30 consists of 16Kb of RAM and 8Kb of EPROM. Memory expansion boards were added to the system to provide additional capacity in EPROM (64Kb) and RAM (64Kb). These Intel boards were combined with the 80/30 to provide an effective combined memory of 56Kb in EPROM and 56Kb in RAM. (The effective added memory (48Kb) is shown in Figure 2.6.1-1.)

The 80/30 card includes a serial RS-232 I/O port which was used to interface to a standard CRT terminal (VT-100, Beehive 100) or host computers for diagnostic and display purposes. An Intel 534 interface card was used to provide another four serial RS-232 ports. For the MFK study, one of these ports was modified to drive a serial RS-422 interface for operation of the LRCU and a set of four switches. This card was planned as the interface between the multibus and the LRCU's to provide the capability of driving up to sixteen PPS units and four LRCU's.

A Sharp thin film electroluminescent (TFEL) panel was used as a scratchpad area. The panel is formatted as a 240 X 320 pixel array. The Sharp panel includes a graphics generation card (Sharp) which was interfaced to the multibus. The graphics card transmits data to the display via a serial RS-422 operating at 300Kb/s.

The luminance sensing and automatic/manual control was achieved by using a photodiode sensor exposed to the ambient light through a filter designed to reduce the

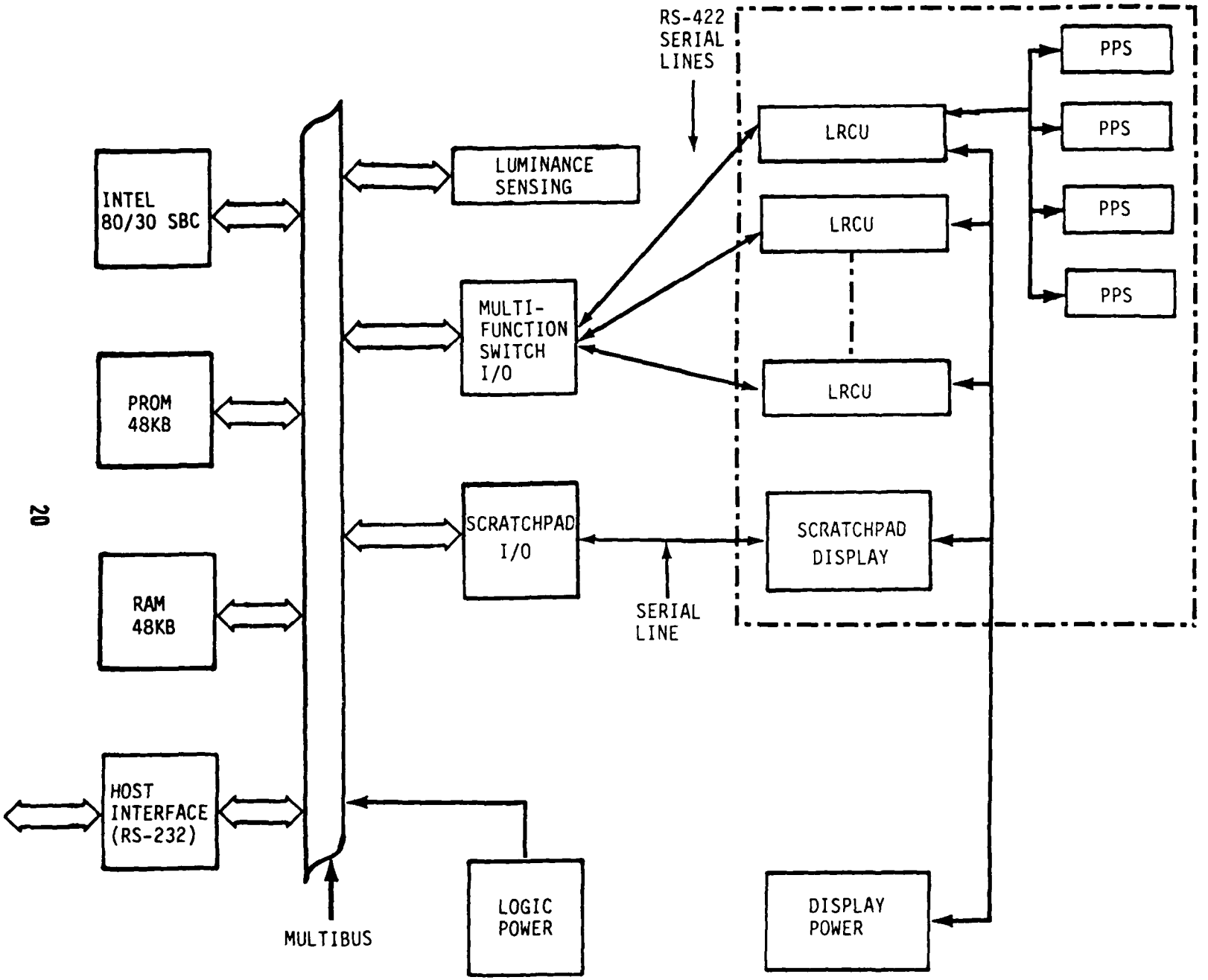


Figure 2.6.1-1. MEK HARDWARE SCHEMATIC

response to near-IR incident light. The sensor output is amplified and a voltage signal is produced for input to an eight bit analog to digital converter. The A/D converter output is interfaced to the multibus. Output from the A/D converter is sampled by the controller operating system which compares it to a table of stored values. The value ranges are linked to the set of available luminance steps in the PPS. The software sends the appropriate value of the luminance step to the LRCU as a luminance control command. The manual control uses a potentiometer to drive an A/D converter which is also sampled by the software. The manual control A/D converter output is used to modify the PPS luminance relative to the automatic setting. A photograph of the MFK controller development system is shown in Figure 2.6.1-2.

2.6.2 SOFTWARE DESIGN

The software design divides the controller software into two major sections. The first is the Operating System which controls the background operation of the MFK and is independent of the data base. The data base (or bases) forms the second major software segment and is specific to a particular application or mission. By dividing the software in this way, the operating system need not be changed to adapt the MFK to different uses. The number of switches used is defined by the data base structure and asumes that the required number of LRCU output ports are available. The controller design used will operate one to 32 switches.

2.6.2.1 OPERATING SYSTEM SOFTWARE

The executive system software is stored in the MFK controller EPROM and controls a number of software modules as shown in Figure 2.6.2.1-1. Upon power-up the MFK Controller performs a system initialization. The initialization includes the following areas:

1) Interrupt structure
2) Baud rate timer
3) Each serial and parallel port
4) All system flags
5) All sytem buffers

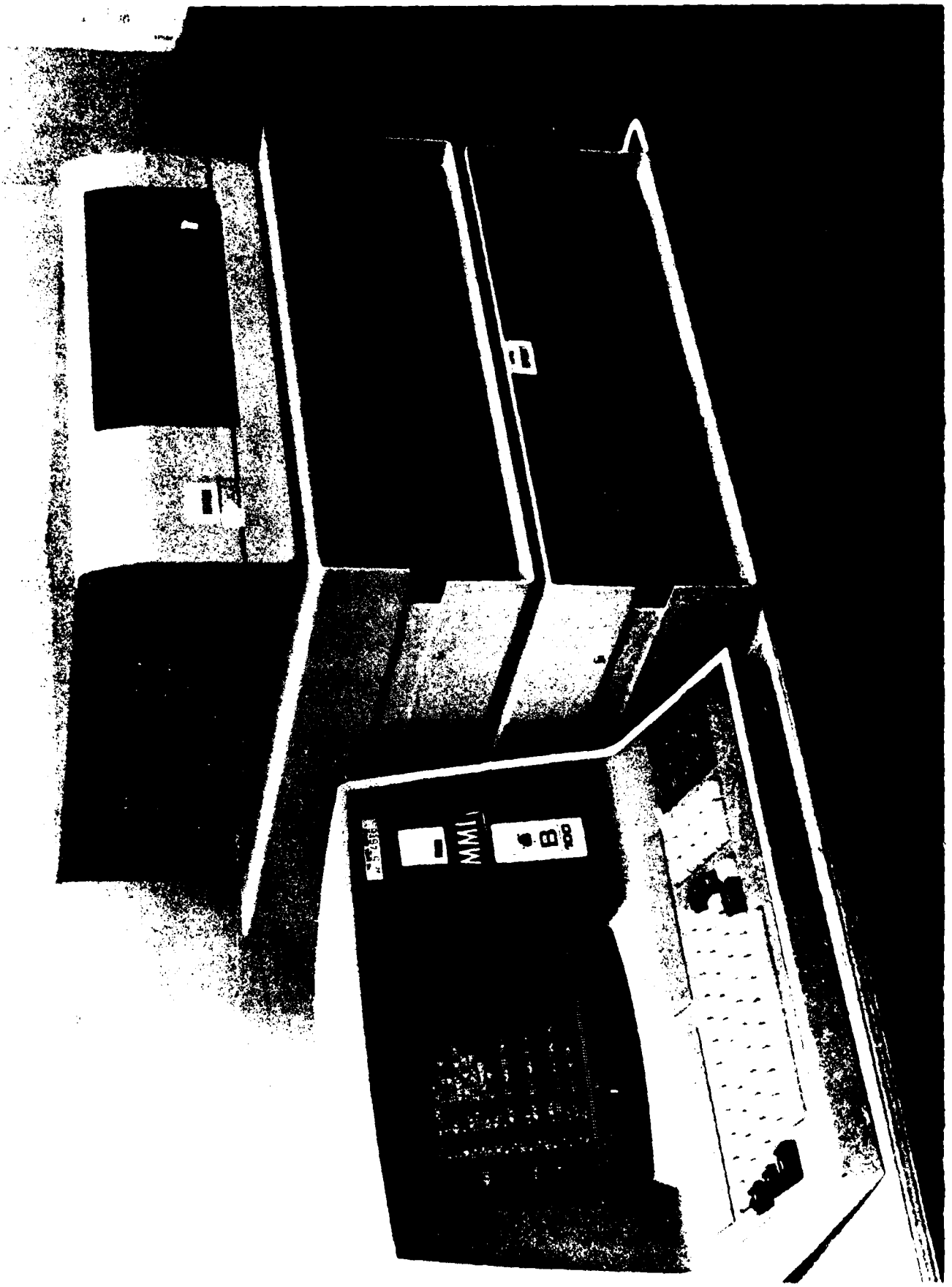


Figure 2.6.1-2: MFK CONTROLLER DEVELOPMENT SYSTEM

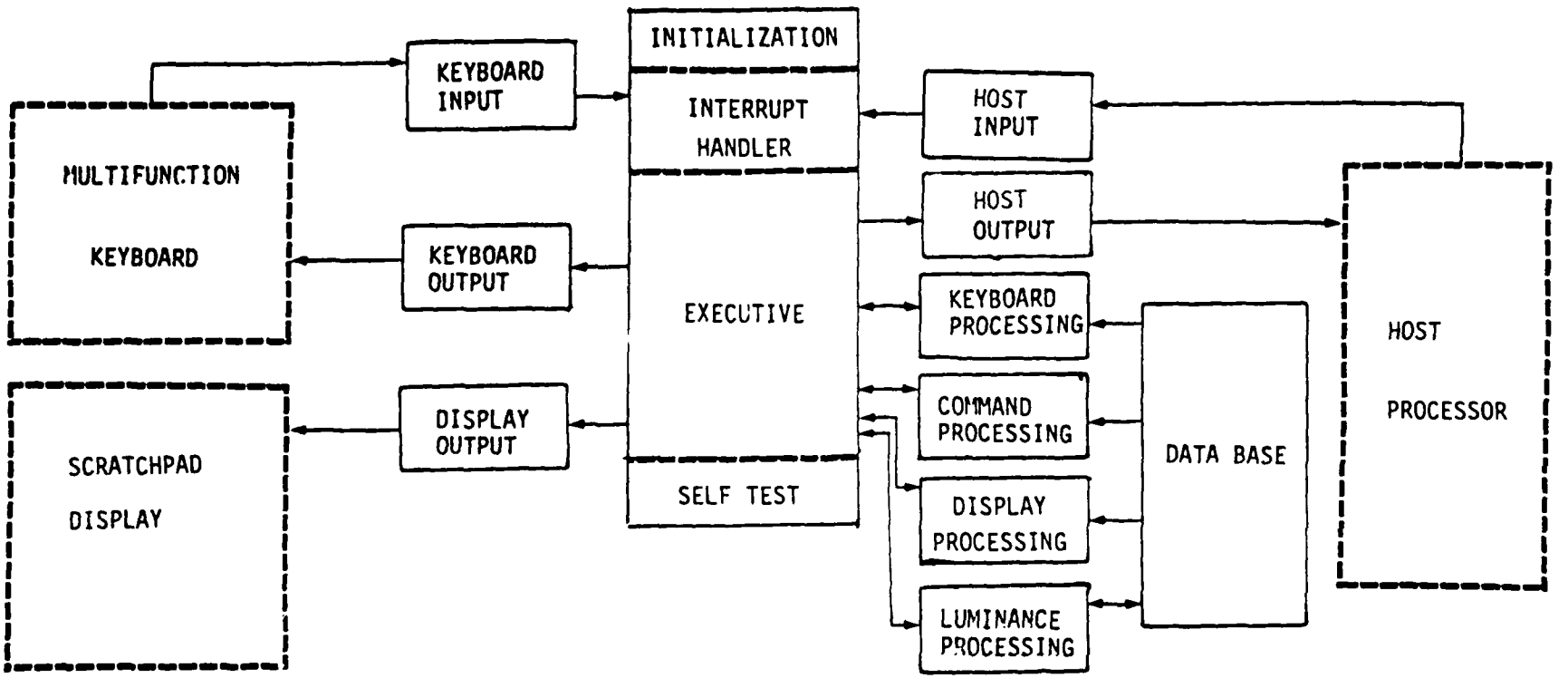


Figure 2.6.2.1-1: MFDCS SOFTWARE BLOCK DIAGRAM

Program control is passed to the system executive following initialization. The executive is responsible for sequencing through the system control modules. A particular control module is called by the executive if its control flag is set. This enables the controller to be event driven and thus respond in a real-time manner. In addition, all inputs and outputs are interrupt driven to ensure that no data or commands are lost.

Each control module is concerned with a specific operation within the MFK operating system. The basic set of control modules includes the following:

Initialization
Page Update
Keyboard Legend Processing
Display Processing
Command Processing
Keyboard Input/output
Host Input/output
Display Output
Luminance Processing
Self-test

The page update module interrogates each memory page that is called by the system for certain information. However, it must first decide what the next page is and then fetch that page. The module then updates the system information and queues the required control modules. For example, when called, it will look to see if the page contains any display information, if so, it notifies display processing which will process the information for display on the scratchpad. Keyboard legend processing updates each legend that the keyboard output routine sends to the keyboard. This operation is always performed each time a switch is depressed by the operator.

Command processing is also called when a switch is depressed. It looks at the current page to see if there are any special commands associated with the specific switch before passing control to the page update module. If a command is found for a switch, command processing queues the appropriate routines to handle the command. Often times this involves both outputs to the scratchpad display and the host. Command

processing is also responsible for interpreting and executing any commands from the host.

Luminance processing is concerned with monitoring the ambient light intensity and correcting the current switch display intensity for any change in the ambient light level.

The keyboard input/output module is responsible for maintaining the communications protocol with the keyboard switches. This is true for the host input and output modules as well. The display outputs are basically simple output drivers.

2.6.2.2 Data Base Software

The data base for the MFK is organized as a series of "pages". The pages are logically linked in hierarchical structure with a top level page leading to a number of second level pages. Pages below the top level can be linked to other pages of the same level, to higher level pages or to lower control level pages. The page format is shown in Figure 2.6.2.2-1. Words listed on the page have the following functions.

1) Word 1 contains the address of the top level page.

2) Word 2 instructs the MFK to anticipate a particular type of switch input.

3) Words 4 and 5 provide information to the MFK on the display processing and location of display data.

4) Switch legend pointers contains the addresses for the keyboard legends associated with this page.

5) Switch next level vectors contain the addresses, of which, one will be selected to be the next page. The page selected is determined by the keyboard switch being depressed.

6) Switch command pointers contain the addresses of the commands associated with this page. When a switch is depressed, the command selected by the switch number is sent to the host.

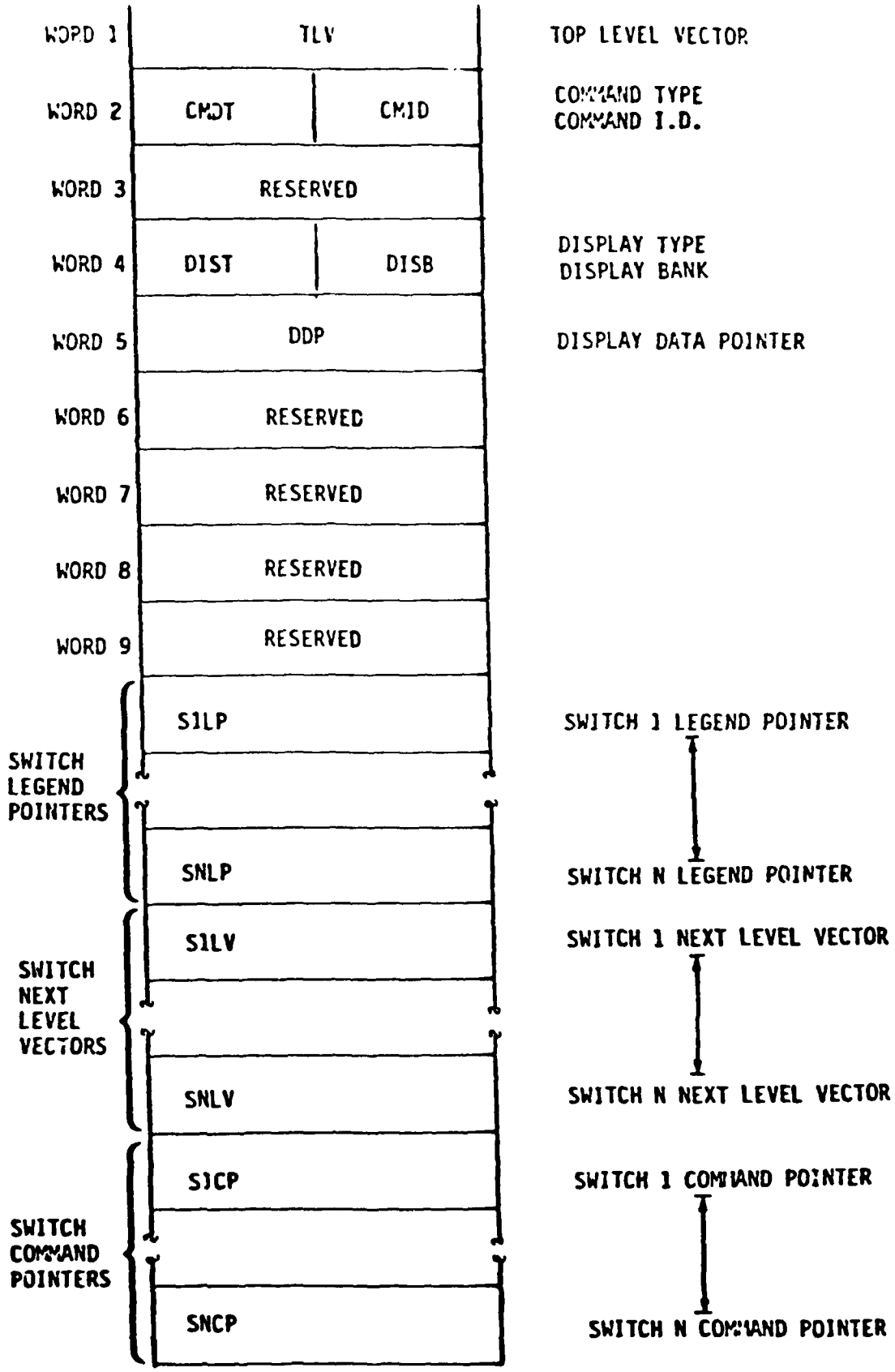


Figure 2.6.2.2-1: DATA BASE PAGE STRUCTURE

This structure provides a standard format for each of the data bases being constructed. This structure is illustrated by the four switch data base in Appendix A.

2.6.3 Logic Refresh and Control Unit and Programmable Pushbutton Switch

The LRCU is a separate board forming the interface between the MFK controller and the PPS units. Each Logic Refresh and Control Unit (LRCU) is capable of driving one to four Programmable Pushbutton Switches (PPS). These switches contain displays consisting of Light Emitting Diodes (LED) mounted in an array 16 rows by 35 columns on 0.025 inch pixel centers (40 lines/inch). The LRCU has on/off control of each of the 560 LED's (pixels) in each of the four PPS's. Each PPS display array can show up to two rows of six characters (5 X 7 pixel font) or one row of three characters (10 X 14 pixel font). Unlimited graphics are also possible as are combinations of characters and graphics. Each PPS also contains a solid state Hall effect switch with tactile feedback.

Figures 2.6.3-1a,b are a block diagram and a functional diagram of the LRCU and PPS. The System Connector provides both LRCU logic power and display power on separate input pins as well as the serial communication link between the LRCU and the user's host computer. Separate fusing and buffering for each PPS are provided on the LRCU board so that even a catastrophic failure of one or more PPS's will not affect normal operation of those remaining.

Commands, data and sumcheck information all enter the LRCU via the RS-422 serial input line, through the system connector, to the Z8 LRCU microprocessor. Each message is validated by the LRCU software prior to taking any action that would destroy existing display information on the PPS's. After a complete message has been received and validated, the microprocessor commands the Custom Refresh Controller (CRC) chip to change from the "refresh mode" to the "write mode". While in the "write mode", all four PPS displays are turned off. The new pixel pattern is then transferred from the microprocessor, through the CRC to the refresh RAM chip, which was specified in the original message. This new pattern could be a complete pattern or just a partial pattern, depending on the amount of data contained in the message. ASCII code character command messages are converted to pixel pattern within the LRCU microprocessor software. Pattern map message (graphics) are simply passed along unchanged from the serial input to the refresh RAM. After completing the

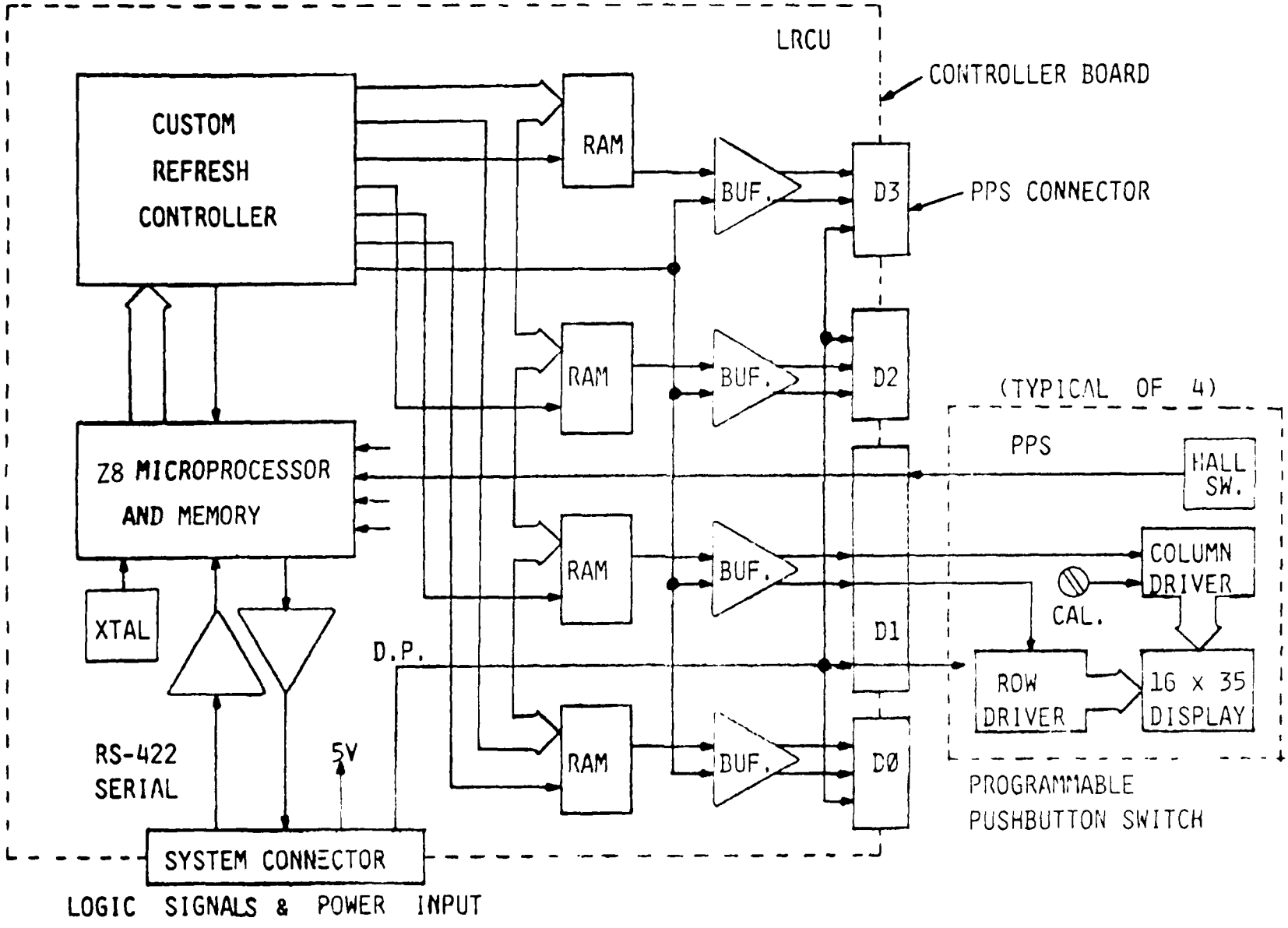


Figure 2.6.3-1a: BLOCK DIAGRAM OF PPS/LRCU UNIT

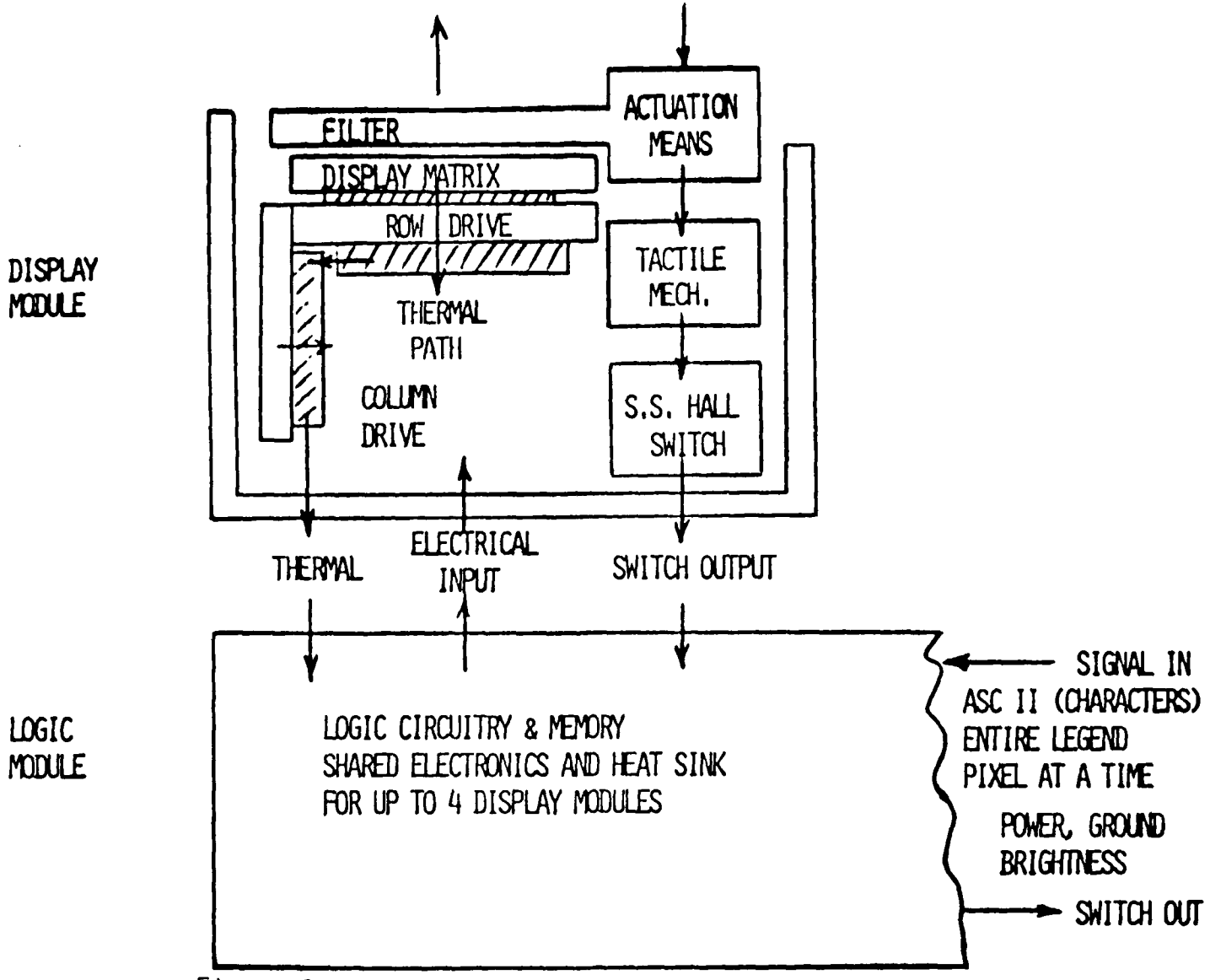


Figure 2.6.3-1b: FUNCTIONAL DIAGRAM OF THE LRCU/PPS UNIT

writing of the new pixel pattern, the microprocessor can switch the CRC back to the "refresh mode", thus turning on all four PPS displays again. It is necessary to turn off all the displays during the "write mode" because the four refresh RAM chips have bussed address lines and because "writing" is done at a much slower rate than display "refreshing" (due to microprocessor speed limitation).

The LRCU system connector is a 15 pin, cannon type DAP-15 PAA and is riveted to the circuit board. The signal interface of this connector meets the requirements of the EIA RS-422 standard. The asynchronous serial communication rate between the LRCU and the host computer is selectable between 2.4K, 4.8K, 9.6K, 19.2Kb/s (see options). The transmission format is the standard 8 bit format shown in Figure 2.6.3-2. No parity bit is used with data recieved by the LRCU. Data bit 7 is odd parity on all transmissions from the LRCU.

2.6.3.1 LRCU Input Messages

The host computer system and controller send messages to the LRCU via the serial data link. These messages are made up of eight bit bytes of information. Figure 2.6.3.1-1 shows the three types of information bytes which are used.

Command Byte

The first byte of any message is a command byte. All command bytes are distinguished by a 1 in bit 7 position. Bits 2 through 6 define the type of command. Bits zero and 1 are generally used to define the PPS number to which the command is directed.

Data Byte

A message may contain anything from zero to 41 data bytes depending on the type of command. All data bytes are distinguised by a zero in bit 7 position. Bits zero through 6 contain the data, which may be an ASCII character, a pixel bit map, luminance value, coordinate position, etc., depending on the type of command.

Sumcheck Byte

All messages end with an "End of Message" command byte followed by a sumcheck byte. This allows the LRCU to verify the validity of the entire message. The

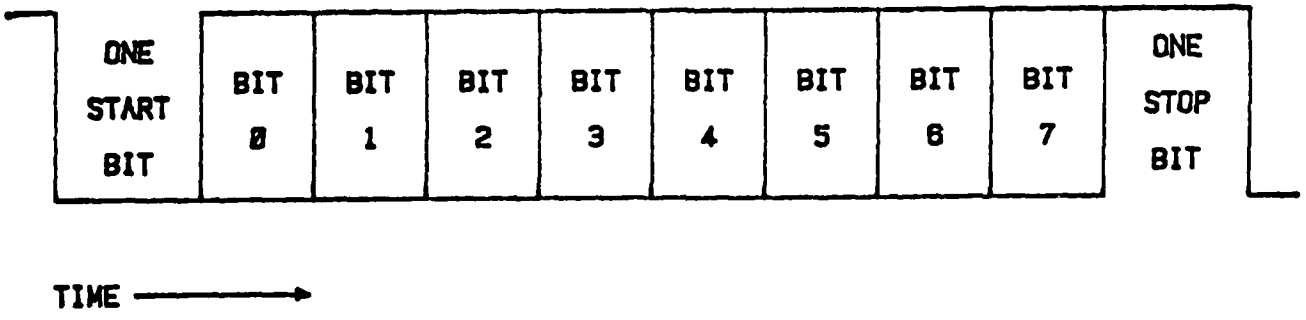
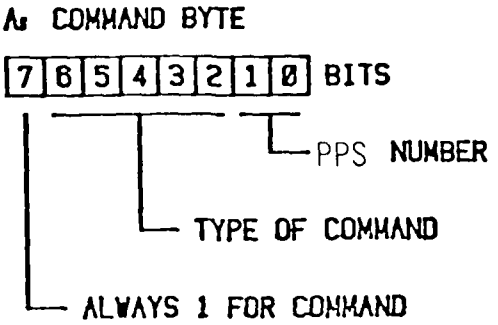
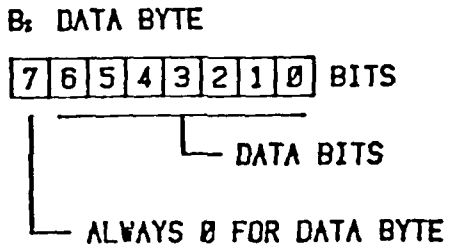


Figure 2.6.3-2: DATA TRANSMISSION FORMAT





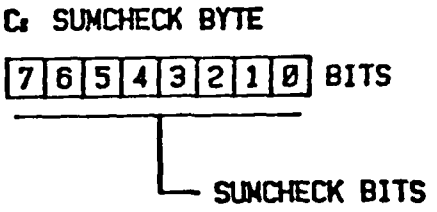


Figure 2.6.3.1-1: INFORMATION BYTE TYPES

sumcheck contains the numerical summation of all of the bytes of the message (carries which occur beyond bit 7 are ignored). As a message is received, the LRCU maintains a running summation of the bytes. The LRCU compares this summation with the sumcheck byte when it is received. The entire message will be rejected by the LRCU if any discrepancy is found in this comparison. No existing information on any of the displays will be changed until a valid sumcheck byte has been received.

Figure 2.6.3.1-2 illustrates the simplest type of message. It consists of only three bytes; that is, two command bytes and a sumcheck byte. The first command byte could be, for example, "Clear Switch Display", or "Blink Switch", or "Self Test", or any of the other commands which require no data. If the command is the type which is directed at only one of the four PPS's, then the PPS number is contained within command byte No. 1. The second command byte is always an "End of Message" command. The third and last byte of the message is the sumcheck byte which is the arithmetic summation of the two previous bytes.

A data message is illustrated in Figure 2.6.3.1-3. It contains a block of data between the two command bytes. The first command byte defines the type of message and the PPS number to which the data is directed. Following this is one or more bytes of data. The "End of Message" (Command No. 2) signals the LRCU that all of the data has been transmitted and that the next byte will be the sumcheck byte.

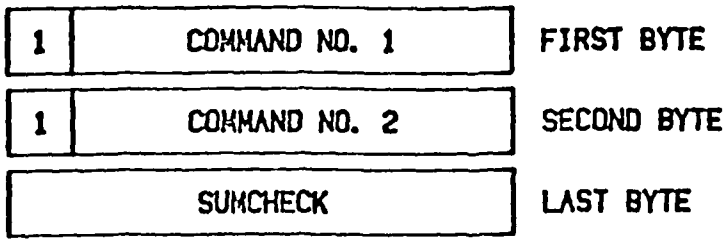
Figure 2.6.3.1-4 through 2.6.3.1-9 are more detailed illustrations of all of the different message types. The following paragraphs describe the function of each of the input message types.

In all messages, bits zero and one (B_0 and B_1) of the "End of Message command are not used by the LRCU. These bits may be used by the host computer to assist in data base management.

SELF TEST, CLEAR DISPLAY, CLEAR ERROR, END OF TRANSMISSION and RETRANSMIT messages (See Figure 2.6.3.1-4)

The above messages follow the format of Figure 2.6.3.1-2 and are located in the command No. 1 position. The LRCU program initiates the action requested by the command as follows:

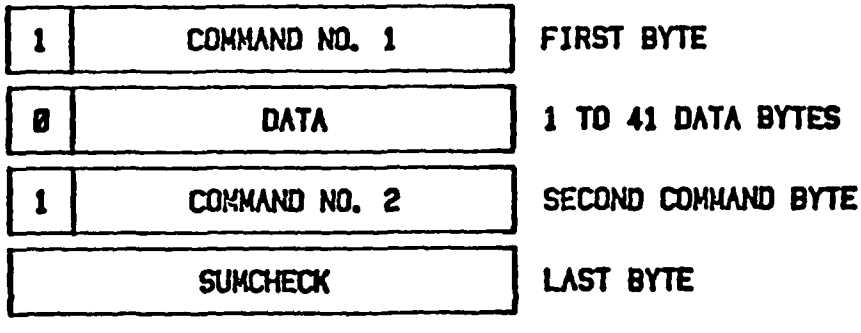
COMMAND ONLY TYPE MESSAGE



SUMCHECK = COMMAND 1 + COMMAND 2

Figure 2.6.3.1-2: THREE BYTE MESSAGE ILLUSTRATION

COMMAND AND DATA TYPE MESSAGE



SUMCHECK = COMMAND 1 + DATA + COMMAND 2

Figure 2.6.3.1-3: DATA MESSAGE FORMAT

1	C_5	C_4	C_3	C_2	C_1	Ø	Ø	COMMAND NO. 1
1	Ø	Ø	Ø	Ø	Ø	X	X	END OF MESSAGE
S_7	S_6	S_5	S_4	S_3	S_2	S_1	$S_Ø$	MESSAGE SUMCHECK

NOTE: X = DON'T CARE BIT

COMMAND BITS

C_5	C_4	C_3	C_2	C_1	
Ø	Ø	Ø	1	Ø	- SELF TEST COMMAND
Ø	Ø	Ø	1	1	- CLEAR DISPLAY COMMAND
1	Ø	1	Ø	Ø	- CLEAR ERROR COMMAND
1	Ø	Ø	Ø	Ø	- END OF TRANSMISSION
1	Ø	Ø	Ø	1	- RETRANSMIT COMMAND

Figure 2.6.3.1-4: COMMAND ONLY MESSAGE FORMATS

1	C_5	C_4	C_3	C_2	C_1	D_1	D_0	COMMAND NO. 1
1	0	0	0	0	0	X	X	END OF MESSAGE
S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	MESSAGE SUMCHECK

NOTE: X = DON'T CARE BIT

COMMAND BITS

C_5 C_4 C_3 C_2 C_1

0 0 1 0 0 - BLINK SWITCH COMMAND

0 0 1 1 0 - CLEAR SWITCH COMMAND

1 0 1 0 1 - STOP BLINK SWITCH COMMAND

SWITCH ADDRESS BITS

D_1 D_0

0 0 - SWITCH 0

0 1 - SWITCH 1

1 0 - SWITCH 2

1 1 - SWITCH 3

Figure 2.6.3.1-5: CLEAR, BLINK, STOP BLINK MESSAGE FORMAT

1	C_5	C_4	C_3	C_2	C_1	D_1	D_0	COMMAND NO. 1
0	X	X	H_4	H_3	H_2	H_1	H_0	'X' COORDINATE
0	X	X	X	V_3	V_2	V_1	V_0	'Y' COORDINATE
0	X	A_5	A_4	A_3	A_2	A_1	A_0	N BYTES OF ASCII DATA
1	0	0	0	0	0	X	X	END OF MESSAGE
S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	MESSAGE SUMCHECK

NOTE: X = DON'T CARE BIT

COMMAND BITS

C_5 C_4 C_3 C_2 C_1

0 0 0 0 1 - 5X7 FONT CHARACTER COMMAND; N < 7

0 1 0 1 0 - 10X14 FONT CHARACTER COMMAND; N < 4

SWITCH ADDRESS BITS

D_1 D_0

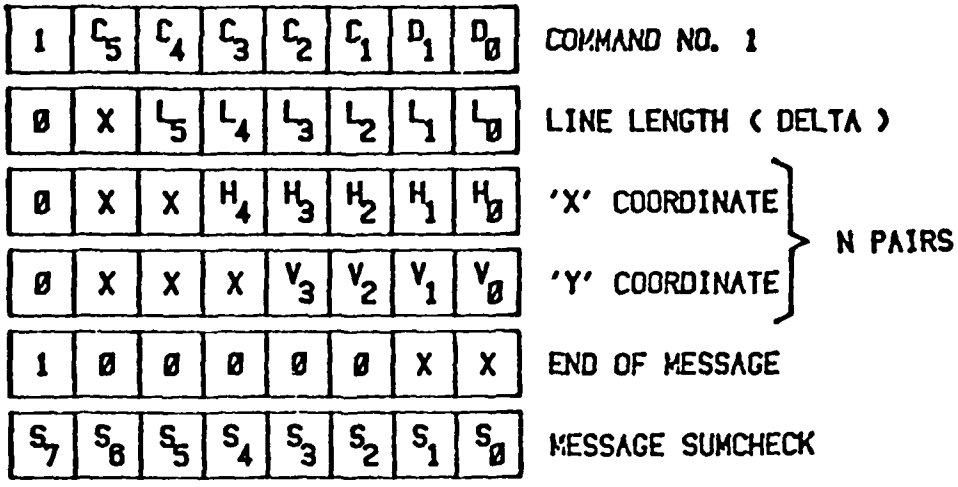
0 0 - SWITCH 0

0 1 - SWITCH 1

1 0 - SWITCH 2

1 1 - SWITCH 3

Figure 2.3.6.1-6: CHARACTER INPUT MESSAGE FORMAT



NOTE: X = DON'T CARE BIT
NOTE: 0 < N < 16

COMMAND BITS

C_5 C_4 C_3 C_2 C_1

0 0 1 1 1 - HORIZONTAL BIT MAP COMMAND

0 1 0 0 0 - VERTICAL BIT MAP COMMAND

SWITCH ADDRESS BITS

D_1 D_0

0 0 - SWITCH 0

0 1 - SWITCH 1

1 0 - SWITCH 2

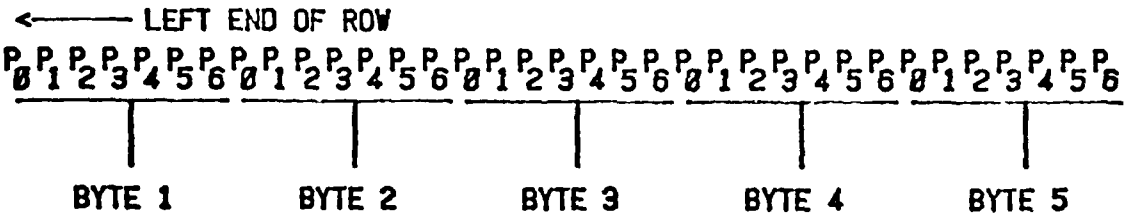
1 1 - SWITCH 3

Figure 2.6.3.1-7: BIT MAP INPUT MESSAGE FORMAT

1	0	1	0	1	1	D_1	D_0	PATTERN MAP COMMAND
0	X	X	X	V_3	V_2	V_1	V_0	'Y' COORDINATE
0	P_6	P_5	P_4	P_3	P_2	P_1	P_0	N X 5 PIXEL PATTERN BYTES
1	0	0	0	0	0	X	X	END OF MESSAGE
S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	MESSAGE SUMCHECK

NOTE: X = DON'T CARE BIT
NOTE: N = NUMBER OF PATTERN ROWS; N < 9

BIT PLACEMENT FOR EACH PIXEL ROW



SWITCH ADDRESS BITS

D_1 D_0

0 0 - SWITCH 0
0 1 - SWITCH 1
1 0 - SWITCH 2
1 1 - SWITCH 3

Figure 2.6.3.1-8: PATTERN MAP INPUT MESSAGE

1	0	1	1	1	1	0	0	LUMINANCE COMMAND
0	X	X	X	X	X	X	X	OPTIONAL BYTE
0	L_6	L_5	L_4	L_3	L_2	L_1	X	LUMINANCE DATA
1	0	0	0	0	0	X	X	END OF MESSAGE
S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	MESSAGE SUMCHECK

NOTE: X = DON'T CARE BIT

LUMINANCE DATA

L_6	L_5	L_4	L_3	L_2	L_1	
1	1	1	1	1	1	- MAXIMUM
.					.	
.					.	37 STEPS
.					.	
0	1	1	0	1	1	- MINIMUM
0	1	1	0	1	0	- OFF
.					.	
.					.	ALWAYS OFF
.					.	
0	0	0	0	0	0	- OFF

Figure 2.6.3.1-9: LUMINANCE CONTROL INPUT MESSAGE

SELF TEST - This command tells the LRCU to perform a series of internal tests and report back with the results (see LRCU output messages). These tests will verify the proper operation of the LRCU microprocessor, ROM memory, RAM memory, timers, the custom Refresh Controller I.C., all four refresh RAM I.C.'s and all four PPS switch outputs. This command destroys all data in the refresh RAM's, therefore all four displays will be blank after this command is invoked. Any PPS's that were in the blinking mode will be returned to non-blinking by this command.

CLEAR DISPLAY - This command tells the LRCU program to clear all four refresh RAM memories thus resulting in all displays being blanked.

CLEAR ERROR - This command tells the LRCU program to clear its internal error flag (which may have been set by a previous sumcheck error, for example) and get ready for a new command. The Clear Error may also be used to abort a partial message (for example an emergency situation which caused a host computer interrupt) and put the LRCU program back into the command input mode. The Clear Error command does not change any current information on any of the displays.

END OF TRANSMISSION - This command tells the LRCU program to enable (turn on) all four displays. The End of Transmission command does not change any current information on any of the displays.

RETRANSMIT - This command tells the LRCU to repeat its last transmission because that transmission contained in parity error or some other problem. The LRCU will retransmit all information, including "Switch Depressed" messages that were transmitted since receiving the last previous valid message. The Retransmit command does not change any current information on any of the displays.

CLEAR SWITCH, BLINK SWITCH and SWITCH BLINK SWITCH messages, (see Figure 2.6.3.1-5)

The above messages follow the format of Figure 2.6.3.1-2. These are non-data messages which are directed to only one of the four PPS's on the LRCU. Command No. 1, therefore, must contain the PPS address as shown in Figure 2.6.3.1-5. The LRCU initiates the action requested by the command as follows.

CLEAR SWITCH - This command tells the LRCU to clear (blank) the refresh memory of the PPS addressed by the command. The contents of the other three refresh memories are not changed.

BLINK SWITCH - This command tells the LRCU program to start blinking the display of the PPS addressed by the command. This blinking occurrs at 1.5Hz and the PPS remains in the blink mode until a Stop Blink or a Self Test message is received. This message does not change any current information on any of the displays.

STOP BLINK SWITCH - This command tells the LRCU program to stop blinking the display of the PPS addressed by the command. This message does not change any current information on any of the displays.

CHARACTER INPUT MESSAGE

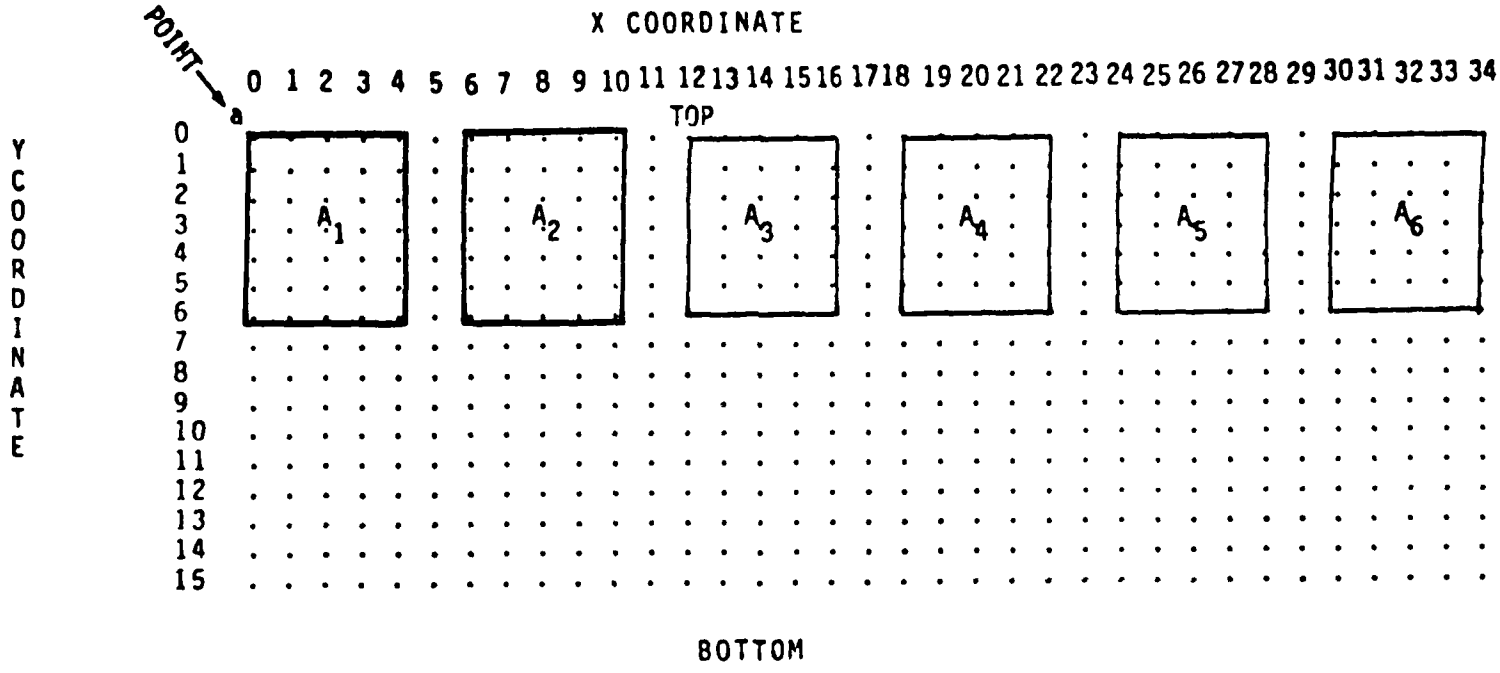
The character input message follows the format of Figure 2.6.3.1-3 and is shown in detail in Figure 2.6.3.1-6. Command No. 1 defines the font size of the characters and the address of the PPS on which the characters are to be displayed.

The next byte of the message, following Command No. 1 is the X coordinate. This binary number could be anything from zero through 34 and it defines the number of unused (unchanged) pixel columns to the left of the first character (see Figure 2.6.3-.1-10).

The third byte (second data byte) of the message is the Y coordinate. This binary number could be anything from zero through 15 and it defines the number of unused (unchanged) pixel rows above the top of the characters (see Figure 2.6.3.1-10).

ASCII character data begins with the fourth byte of the message (third data byte). One to six characters may be included in one message (one to three characters for a 10 by 14, font command). Following the last character, the End of Message command signals the LRCU that the data has ended and the next byte will be the Sumcheck.

Two separate character messages are required to produce two lines of characters on the same display. Generally a Clear Display or Clear Switch command would be used



NOTE: 5 x 7 Character font shown for six positions

Figure 2.6.3.1-10: LED SWITCH MATRIX

to erase old data from a display prior to receiving a new Character Message. It is possible, however, to change only selective characters within existing patterns by inputting the new characters with the proper coordinates. Each character erases the existing pixel pattern within the 5 by 7 pixel area of the character and also the 7 pixels in the column adjacent to the left side of the character area. Single line messages may be centered vertically in the display area. Superscripts and subscripts are possible with proper use of coordinates.

BIT MAPPING HORIZONTAL & VERTICAL

Bit Mapping messages allow the user to draw straight lines either horizontally or vertically. These lines may begin at any pixel location (x and Y coordinates) and extend for any length (delta). From one to fifteen parallel lines may be drawn by a single message provided the lines all have the same length. No problems will be incurred if lines are specified by the message will be turned on but no other pixels will be changed.

Bit Mapping messages follow the format of Figure 2.6.3.1-3 and are shown in detail in Figure 2.6.3.1-7. Command No. 1 defines the type of bit mapping message (horizontal or vertical) and the address of the PPS to which the message is directed. The next byte of the message, following command No. 1, is the pixel length of the line to be drawn (number of pixels to be turned on). An error response will result if this byte is zero or greater than 63.

The following data bytes consist of one or more X-Y coordinate pairs which fix the top pixel of vertical lines or the left end pixel of horizontal lines. Up to fifteen coordinate pairs (thirty bytes) may be included in a single message. Following the last coordinate, the End of Message signals the LRCU that the coordinate data has ended and the next byte will be the Sumcheck. Bit Mapping messages provide a convenient means for underlining and overlining or for drawing complete boxes around words as an attention getter.

PATTERN MAPPING

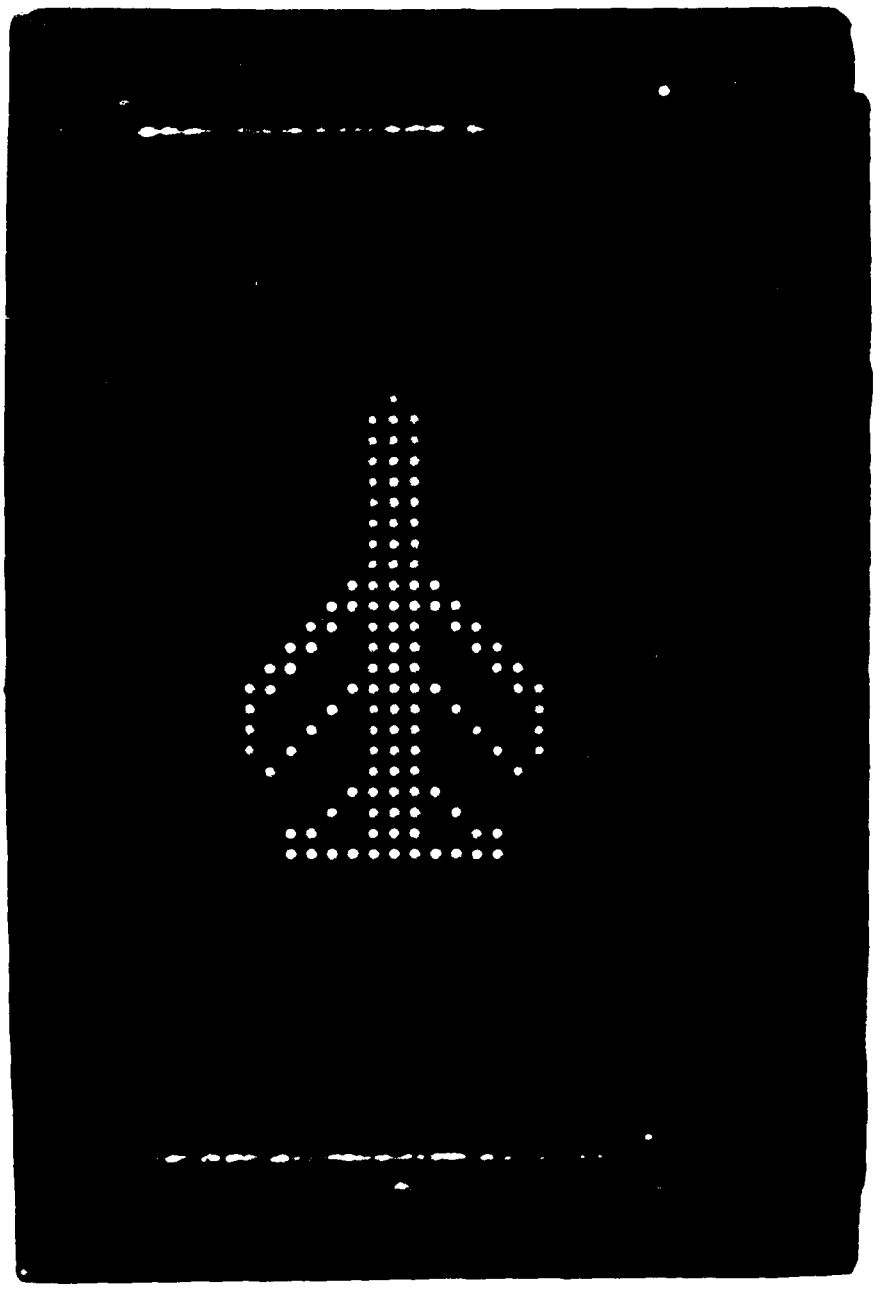
Pattern Mapping messages allow the user to have independent on/off control of each pixel of the display. This allows the display of any possible pattern within the limits of

the 16 X 35 pixel format (see for example Figure 2.6.3.1-11). The pattern map is specified on a row by row basis with five consecutive data bytes (seven bits used in each byte) needed for each pixel row. Pixel data bytes would be required to fill a complete display of 16 pixel rows. It is not possible, however, for a single pattern map message to fill the complete display. A single pattern map message may be used to fill any number of consecutive pixel row from one row to eight rows.

Pattern Mapping messages follow the format of Figure 2.6.3.1-3 and are shown in detail in Figure 2.6.3.1-8. Command No. 1 defines the pattern mapping command and the PPS to which the message is directed. The next byte of the message is the Y coordinate which defines the first (top) pixel row of the pattern. Pixel pattern data begins with the third byte of the message. Pixel data must be in multiples of five bytes up to a maximum of forty bytes. All existing display data within a row used by a pattern map message will be lost and replaced with the new pattern map. If character and/or Bit Map data is desired in the same pixel row as a pattern map, then the pattern map should be transmitted first, followed by the Character message, followed by the Bit Map message. The End of Message command signals the LRCU that the pattern map data has ended and that the next byte will be the Sumcheck.

LUMINANCE CONTROL MESSAGE

The luminance input message follows the format of Figure 2.6.3.1-3 and is shown in detail in Figure 2.6.3.1-9. This message controls the luminance (brightness) of all four PPS displays. Command No. 1 defines the Luminance Control command which is never directed toward a particular PPS address (bit zero and one are always zeros). Following command No. 1 there may be one or two data bytes which specify the luminance value. If more than one data byte is received, only the last (most significant) byte will be used. Bit zero of the last byte is a "don't care" bit. Bits one through 6 control the relative luminance as shown in Figure 2.6.3.1-9. If these six bits (L_9 through L_{14}) are all 1's, the display will be at maximum brightness. Other luminance settings are as follows:



L_{14}	L_{13}	L_{12}	L_{11}	L_{10}	L_9		
1	1	1	1	1	1	Max.	
					.		
					.		37 Steps
					.		
0	1	1	0	1	1	Min.	
0	1	1	0	1	0		
					.		
					.		Displays Off
					.		
0	0	0	0	0	0		

2.6.3.2 LRCU Output Messages

The message structure for communication from the LRCU to the controller is given in Figure 2.6.3.2-1. The most significant bit, "P", in each message is a parity bit set to give odd parity for the total of the 8 bits.

RETRY Message (Figure 2.6.3.2-1, No. 1)

If the message received by the LRCU is declared invalid for any one of a number of reasons, the LRCU will respond by sending a RETRY message. The LRCU at this time, will not accept anymore messages until a CLEAR ERROR command has been received. THe LRCU will, however, respond to a valid RETRANSMIT command by retransmitting the RETRY message. The two least significant bits (RO and R1) of the RETRY message will indicate the type of error which occurred in the received message.

LRCU OUTPUT MESSAGES

7	6	5	4	3	2	1	0	BITS
P	0	0	1	0	0	0	0	'ACKNOWLEDGE'
P	0	0	0	0	0	R_1	R_0	'RETRY'
P	0	0	0	0	1	0	0	'SELF TEST PASSED'
P	0	1	0	F_1	F_0	A_1	A_0	'SELF TEST FAILED'
P	0	0	0	1	1	D_1	D_0	'SWITCH DEPRESSED'

NOTE: P = ODD PARITY BIT

SWITCH ADDERSS BITS

D_1	D_0	
0	0	- SWITCH 0
0	1	- SWITCH 1
1	0	- SWITCH 2
1	1	- SWITCH 3

Figure 2.6.3.2-1: LRCU OUTPUT MESSAGE FORMAT

R_1	R0	Error Type
0	0	Command No. 1 Error
0	1	Data Error or EOM Error
1	0	Sumcheck Error
1	1	Coordinate Error

SELF TEST PASS (Figure 2.6.3.2-1)

This response to a SELF TEST COMMAND message indicates the successful completion of the self testing program, in the LRCU, with no errors being detected.

SELF TEST FAILED (Figure 2.6.3.2-1 No. 3)

This response to a SELF TEST COMMAND message indicates the detection of an error by the self testing program in the LRCU. Bits A_0, A_1, F_0, F_1, indicate the type of error which occurred.

The Failure Codes and Abort Codes are as follows:

A. Failure Code A (FF=00)
   1. Abort Code 1 - Not used.
   2. Abort Code 2 - ROM Failure
   3. Abort Code - RAM Failure
   4. Abort Code 4 - Refresh Controller Chip Failure.

B. Failure Code B (FF=01)
   Switch output failure; Abort Code indicates PPS number.

C. Failure Code C (FF=10)
   Refresh memory failure; Abort Code indicates PPS number.

D. Failure Code D
   Not used.

SWITCH DEPRESSED (Figure 2.6.3.2-1 No. 4)

Upon actuation of any one of the PPS switches, the LRCU will transmit a SWITCH DEPRESSED message. The S0 and S1 bits of this message define which of the four switches was depressed. This message will only be transmitted while the LRCU is in the Command No. 1 input waiting mode. That is, it will not transmit this message while in the process of receiving a message. If quicker response to switch actuations is required by the customer, the "Interrrupt Request Output" (see LRCU schematic) can be monitored by the customer. A five millisecond pulse will occur on this output no more than five milliseconds after the switch actuation. Software in the host computer could then abort the message being transmitted, causing the LRCU to return to the input wait loop. The LRCU would then transmit the SWITCH DEPRESSED code (see CLEAR ERROR input message).

ACKNOWLEDGE

The LRCU will transmit the ACKNOWLEDGE message after completing the task called for by the message that was received. The ACKNOWLEDGE message signals the host computer that the LRCU is ready for the next command.

Message Examples

Example #1

Suppose it is required to clear the refresh RAM's for all four PDP's so that a completely new set of display messages can be loaded.

The following message sequence would be transmitted to the LRCU:

Byte No.	Transmitted Bits 7	6	5	4	3	2	1	0	Comments
1	1	0	0	0	1	1	0	0	"Clear Display" Command
2	1	0	0	0	0	0	0	0	End of Message Command
3	0	0	0	0	1	1	0	0	Sumcheck

After the RAM's have been erased, the LRCU with respond with an "Acknowledge" code.

Example #2

Suppose the following message is required on PDP number zero.

It is further required that this word be displayed in 10 by 14 font. First, a "Clear Switch" or "Clear Display" command message would be used to clear any previous display pattern from the refresh RAM (see Example #1). Then the following message would be transmitted to the LRCU:

Byte No.	Transmitted Bits 7	6	5	4	3	2	1	0	Comments
1	1	0	1	0	1	0	0	0	10 x 14 Font Command to PDP #0
2	0	0	0	0	0	0	0	0	X Coordinate is 0
3	0	0	0	0	0	0	0	1	Y Coordinate is 1
4	0	1	0	1	0	0	1	0	ASCII Code for "R"
5	0	1	0	1	0	1	0	1	ASCII Code for "U"
6	0	1	0	0	1	1	1	0	ASCII Code for "N"
7	1	0	0	0	0	0	0	0	End of Message Command
8	0	0	0	1	1	1	1	0	Sumcheck

Example #3

Suppose the following message is required on PDP number 3:

It is further required that this single line message be centered, both horizontally and vertically within the display area. The refresh RAM should be erased as in the previous examples. Then the following message would be transmitted to the LRCU:

Byte No.	Transmitted Bits 7	6	5	4	3	2	1	0	Comments
1	1	0	0	0	0	1	1	1	5 x 7 Font Command to PDP #3
2	0	0	0	0	0	1	1	0	X Coordinate is 6
3	0	0	0	0	0	1	0	1	Y Coordinate 5
4	0	1	0	1	0	0	1	1	ASCII Code for "S"
5	0	1	0	1	0	1	0	0	ASCII Code for "T"
6	0	1	0	0	1	1	1	1	ASCII Code for "O"
7	0	1	0	1	0	0	0	0	ASCII Code for "P"
8	1	0	0	0	0	0	0	0	"End of Message" Command
9	0	1	0	1	1	0	0	0	Sumcheck

The above message will result in the word "STOP" approximately centered in the display.

Example #4

Suppose the following message is required on PDP number 2:

It is further required that this two line message be centered in the display area. The refresh RAM would first be cleared as described in Example #1.

Since the required message is composed of two rows of characters, two separate message sequences must be transmitted to the LRCU, as shown below.

First message sequence:

Byte No.	Transmitted Bits 7	6	5	4	3	2	1	0	Comments
1	1	0	0	0	0	1	1	0	5 x 7 Font Command to PDP #2
2	0	0	0	0	1	0	0	0	X Coordinate is 8
3	0	0	0	0	0	0	0	0	Y Coordinate is 0
4	0	1	0	1	0	1	1	0	ASCII Code for "V"
5	0	1	0	0	1	0	0	0	ASCII Code for "H"
6	0	1	0	0	0	1	1	0	ASCII Code for "F"
7	1	0	0	0	0	0	0	0	"End of Message" Command
8	1	1	1	1	0	0	1	0	Sumcheck

Second message sequence:

1	1	0	0	0	0	1	1	0	5 x 7 Font Command to PDP #2
2	0	0	0	0	1	1	1	0	X Coordinate is 14
3	0	0	0	0	1	0	0	1	Y Coordinate is 9
4	0	0	1	1	0	0	0	1	ASCII Code for "1"
5	1	0	0	0	0	0	0	0	"End of Message" Command
6	0	1	0	0	1	1	1	0	Sumcheck

It makes no difference which of the above sequences is transmitted first.

3.0 SWITCH/DISPLAY MODULE EVALUATION

The PPS/LRCU modules were developed as a first step toward a completely self-contained programmable legend switch. As such, they do not, at present, have all the desired features for such a switch. One of the goals of this study is the determination of the areas in which the present design is satisfactory and those areas in which improvements are needed in the next model. Evaluation of the switch/display modules was conducted on representative samples of individual displays and on complete switch units. The following subsections describe those test procedures and some of the results obtained.

3.1Display Parameter Measurements and Evaluations

Display parameters were measured to establish the performance of a representative sample of the 16 X 35 LED matrices received from Optotech.

3.1.1 Luminance Characteristic Measurements

A number of different measurements were made to define the luminance characteristics of the displays. The procedures for and results of these measurements are described in the following subsections.

The display units were placed without filter, in a prober that provided all electrical connections from row and column drivers. The prober with the LED matrix unit was installed in a dark, non-reflective enclosure as shown in Figure 3.1.1-1. Within that enclosure, a sensor was aligned with the center normal of the display and aimed at the display center. The distance between display center and sensor should not be less than ten times the larger of the active display diagonal (largest dimension) and the active sensor diagonal. For the sensor, any detector/amplifier or detector with separate amplifier may be used that has enough response at the LED emission wavelengths to provide a satisfactory signal-to-noise ratio, and of which the output signal is proportional to the luminous exitance of the radiating sources. Examples of satisfactory detector/amplifiers are the UDT 500D and the UDT 555D.

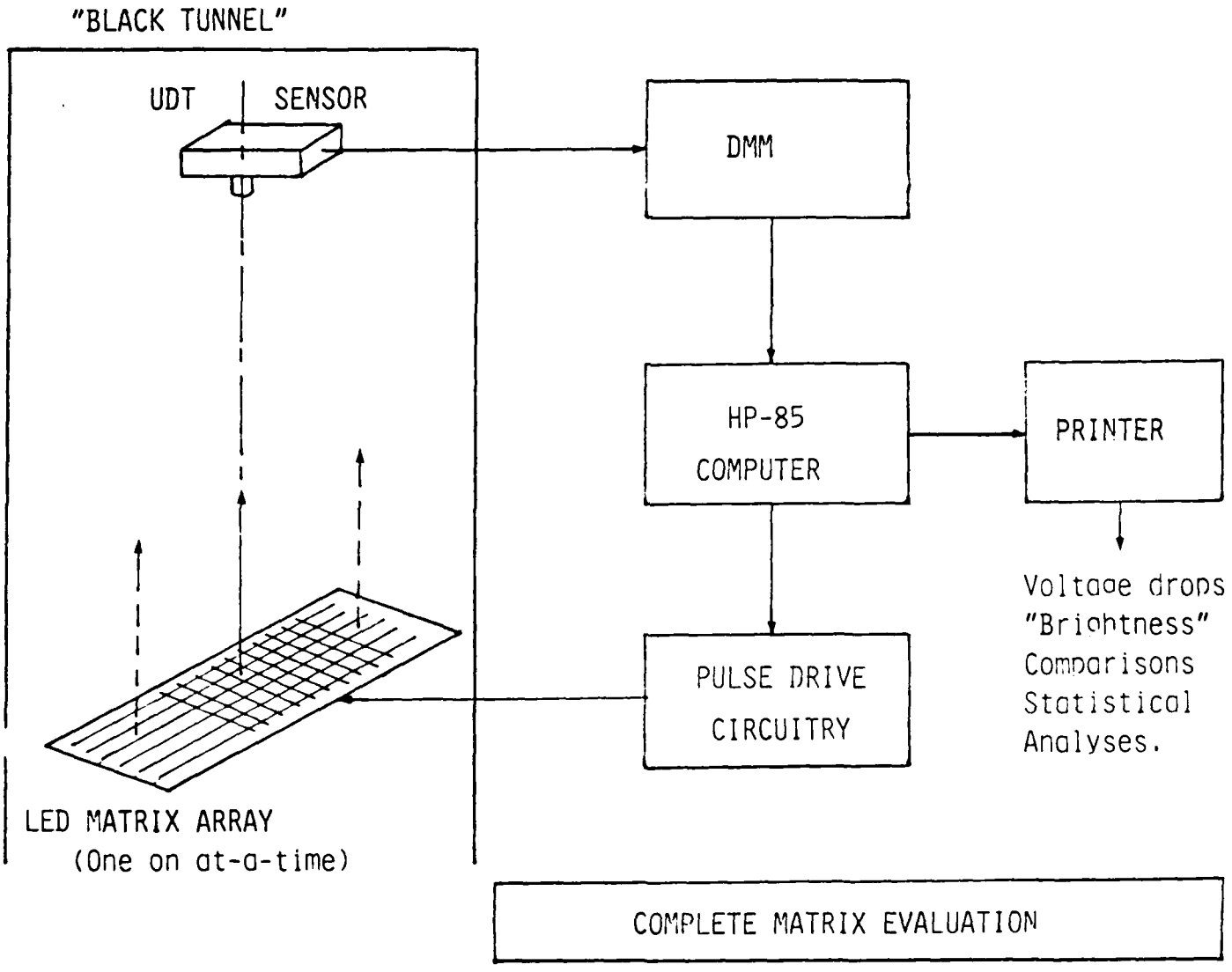


Figure 3.1.1-1: PIXEL LUMINANCE TEST SET

The output of the sensor-amplifier was connected via a digital multimeter with computer interface (Fluke 8860A) to a HP85 processing computer. With proper programming this computer drives the pulse drive circuitry for the display unit so that only one pixel is on at a time; it also receives and processes the data from the sensor and from the drive circuitry, such as the forward voltage for each pixel at a constant forward current such as 10mA DC, and it stores the received data in memory in matrix form. Via additional programming these data were processed and the results provided on a display screen and to a printer for a permanent record.

Drive cycles were provided as follows. After a previous pixel was turned off, a 200 msec. waiting period was provided by programming. The continuous UDT sensor response (all pixels off) was sampled and the value stored in the computer (e.g., call this $U_f(x,y)$). The next pixel on was then turned on and after another 200 msec. delay (for stabilization) the sensor output (e.g. $U_n(x,y)$) was sampled and stored. Then this pixel was turned off, which completed one pixel cycle. Afterwards, via another program, a new matrix was obtained showing for each pixel $U_n(x,y) - U_f(x,y)$. This was printed out as shown in Table 3.1.1-1, by (column, row) number; the values represent the relative luminous exitance of all the pixels. Each pixel was driven at 10 ma DC.

The computer selects from all the pixel measurements, the three lowest, three highest and six average (or nearest average) pixels over the matrix array. These pixels are then measured using a Pritchard photometer to normalize the raw pixel measurements to photometric unit measurements (fL). For Sample 167 shown in Table 3.1.1-1, the average display luminance was 1949 fL. Three other display units averaged 2075 fL. These values were obtained with zero ambient light, no filter over the display, and 10ma DC drive current per pixel. Luminance uniformity for the complete displays is inspected and adjusted using a trim potentiometer on the drive electronics. These adjustment measurements are made at a 6⅛% duty cycle with an average drive current of 1ma and a peak of 16ma. Figure 3.1.1-2 shows the effect of a green filter on the measured luminance of a discrete LED matrix. These measurements were also taken at the 6⅛% duty cycle. All the measurements described above used a 16 mil effective probe diameter with the exception of the relative measurements shown in Table 3.1.1-1.

SAMPLE = 167

(0, 0)	29.1	(0, 1)	31.2	(0, 2)	28.2	(0, 3)	26.9	(0, 4)	26.8	(0, 5)	28.1	(0, 6)	30.2	(0, 7)	32.6				
(0, 0)	29.0	(0, 9)	32.0	(0,10)	31.5	(0,11)	26.9	(0,12)	32.4	(0,13)	33.4	(0,14)	30.9	(0,15)	29.6				
(1, 0)	29.7	(1, 1)	27.6	(1, 2)	25.9	(1, 3)	27.6	(1, 4)	28.9	(1, 5)	29.9	(1, 6)	30.7	(1, 7)	35.6				
(1, 0)	28.9	(1, 9)	28.9	(1,10)	32.3	(1,11)	33.2	(1,12)	32.9	(1,13)	33.5	(1,14)	30.6	(1,15)	29.7				
(2, 0)	25.8	(2, 1)	26.3	(2, 2)	25.2	(2, 3)	25.5	(2, 4)	25.1	(2, 5)	26.0	(2, 6)	26.2	(2, 7)	25.7				
(2, 0)	28.6	(2, 9)	26.6	(2,10)	24.2	(2,11)	25.8	(2,12)	26.5	(2,13)	26.8	(2,14)	25.5	(2,15)	27.2				
(3, 0)	25.7	(3, 1)	24.4	(3, 2)	23.1	(3, 3)	23.3	(3, 4)	23.7	(3, 5)	22.8	(3, 6)	23.8	(3, 7)	18.9				
(3, 0)	28.5	(3, 9)	29.9	(3,10)	31.7	(3,11)	28.2	(3,12)	28.8	(3,13)	28.6	(3,14)	30.7	(3,15)	26.8				
(4, 0)	30.8	(4, 1)	27.9	(4, 2)	29.8	(4, 3)	29.4	(4, 4)	28.2	(4, 5)	28.9	(4, 6)	27.5	(4, 7)	28.4				
(4, 0)	27.5	(4, 9)	27.9	(4,10)	26.6	(4,11)	26.7	(4,12)	26.8	(4,13)	27.8	(4,14)	29.5	(4,15)	30.9				
(5, 0)	28.1	(5, 1)	29.7	(5, 2)	28.7	(5, 3)	26.5	(5, 4)	28.5	(5, 5)	29.2	(5, 6)	27.1	(5, 7)	26.5				
(5, 0)	24.1	(5, 9)	22.8	(5,10)	26.5	(5,11)	27.7	(5,12)	28.5	(5,13)	29.6	(5,14)	28.9	(5,15)	29.9				
(6, 0)	24.6	(6, 1)	24.1	(6, 2)	23.2	(6, 3)	22.8	(6, 4)	22.9	(6, 5)	21.4	(6, 6)	21.6	(6, 7)	20.9				
(6, 0)	21.5	(6, 9)	19.6	(6,10)	21.9	(6,11)	23.1	(6,12)	23.9	(6,13)	24.8	(6,14)	25.6	(6,15)	25.1				
(7, 0)	28.5	(7, 1)	28.9	(7, 2)	28.1	(7, 3)	28.4	(7, 4)	27.4	(7, 5)	26.2	(7, 6)	28.7	(7, 7)	27.2				
(7, 0)	24.4	(7, 9)	24.7	(7,10)	26.2	(7,11)	27.9	(7,12)	27.8	(7,13)	28.9	(7,14)	28.1	(7,15)	27.8				
(8, 0)	25.7	(8, 1)	25.8	(8, 2)	25.1	(8, 3)	25.2	(8, 4)	25.6	(8, 5)	25.4	(8, 6)	27.9	(8, 7)	26.8				
(8, 0)	28.3	(8, 9)	27.2	(8,10)	29.5	(8,11)	26.6	(8,12)	27.5	(8,13)	26.5	(8,14)	28.2	(8,15)	26.5				
(9, 0)	28.8	(9, 1)	29.7	(9, 2)	27.1	(9, 3)	28.5	(9, 4)	28.2	(9, 5)	26.1	(9, 6)	28.1	(9, 7)	29.8				
(9, 0)	25.2	(9, 9)	24.6	(9,10)	25.4	(9,11)	26.1	(9,12)	24.4	(9,13)	26.8	(9,14)	25.1	(9,15)	25.2				
(10, 0)	28.8	(10, 1)	25.8	(10, 2)	22.6	(10, 3)	23.9	(10, 4)	24.7	(10, 5)	24.3	(10, 6)	24.2	(10, 7)	24.2				
(10, 0)	27.7	(10, 9)	27.8	(10,10)	27.8	(10,11)	27.6	(10,12)	28.7	(10,13)	27.8	(10,14)	26.9	(10,15)	28.8				
(11, 0)	28.2	(11, 1)	29.1	(11, 2)	27.5	(11, 3)	29.1	(11, 4)	29.3	(11, 5)	30.8	(11, 6)	30.4	(11, 7)	27.3				
(11, 0)	25.4	(11, 9)	25.9	(11,10)	28.1	(11,11)	27.2	(11,12)	26.7	(11,13)	27.3	(11,14)	27.6	(11,15)	28.7				
(12, 0)	28.8	(12, 1)	28.2	(12, 2)	26.2	(12, 3)	27.5	(12, 4)	25.5	(12, 5)	27.8	(12, 6)	28.6	(12, 7)	28.5				
(12, 0)	28.6	(12, 9)	28.8	(12,10)	28.3	(12,11)	30.6	(12,12)	28.6	(12,13)	27.9	(12,14)	29.9	(12,15)	29.8				
(13, 0)	21.7	(13, 1)	21.1	(13, 2)	22.4	(13, 3)	22.2	(13, 4)	21.8	(13, 5)	21.9	(13, 6)	23.8	(13, 7)	23.6				
(13, 0)	25.9	(13, 9)	23.9	(13,10)	26.8	(13,11)	27.8	(13,12)	27.6	(13,13)	27.2	(13,14)	27.8	(13,15)	29.1				
(14, 0)	26.4	(14, 1)	27.6	(14, 2)	27.2	(14, 3)	23.2	(14, 4)	24.1	(14, 5)	25.8	(14, 6)	22.5	(14, 7)	23.5				
(14, 0)	27.9	(14, 9)	26.8	(14,10)	29.5	(14,11)	28.4	(14,12)	28.2	(14,13)	28.6	(14,14)	26.7	(14,15)	29.2				
(15, 0)	26.6	(15, 1)	24.5	(15, 2)	23.6	(15, 3)	21.8	(15, 4)	23.9	(15, 5)	24.4	(15, 6)	22.7	(15, 7)	23.4				
(15, 0)	28.1	(15, 9)	23.8	(15,10)	27.8	(15,11)	28.8	(15,12)	29.9	(15,13)	27.2	(15,14)	29.6	(15,15)	31.2				
(16, 0)	25.9	(16, 1)	27.9	(16, 2)	21.4	(16, 3)	19.9	(16, 4)	21.3	(16, 5)	23.8	(16, 6)	24.8	(16, 7)	25.8				
(16, 0)	21.8	(16, 9)	22.9	(16,10)	22.5	(16,11)	22.5	(16,12)	20.8	(16,13)	22.7	(16,14)	21.4	(16,15)	25.9				
(17, 0)	23.3	(17, 1)	23.6	(17, 2)	22.6	(17, 3)	20.9	(17, 4)	22.9	(17, 5)	23.2	(17, 6)	22.9	(17, 7)	20.9				
(17, 0)	19.1	(17, 9)	22.7	(17,10)	22.2	(17,11)	21.8	(17,12)	22.6	(17,13)	22.6	(17,14)	24.8	(17,15)	23.3				
(18, 0)	26.2	(18, 1)	23.6	(18, 2)	24.3	(18, 3)	0.4	(18, 4)	23.3	(18, 5)	24.5	(18, 6)	22.7	(18, 7)	23.1				
(18, 0)	21.9	(18, 9)	22.8	(18,10)	23.8	(18,11)	21.5	(18,12)	21.7	(18,13)	22.3	(18,14)	23.1	(18,15)	21.3				
(19, 0)	25.6	(19, 1)	25.9	(19, 2)	24.9	(19, 3)	23.6	(19, 4)	24.2	(19, 5)	25.2	(19, 6)	24.5	(19, 7)	23.2				
(19, 0)	22.3	(19, 9)	20.4	(19,10)	22.7	(19,11)	24.6	(19,12)	25.1	(19,13)	24.9	(19,14)	24.2	(19,15)	23.9				
(20, 0)	25.8	(20, 1)	27.1	(20, 2)	26.3	(20, 3)	24.5	(20, 4)	23.6	(20, 5)	23.5	(20, 6)	21.9	(20, 7)	22.9				
(20, 0)	26.8	(20, 9)	26.8	(20,10)	26.7	(20,11)	26.3	(20,12)	25.9	(20,13)	25.9	(20,14)	27.7	(20,15)	27.8				
(21, 0)	22.9	(21, 1)	22.9	(21, 2)	19.7	(21, 3)	20.1	(21, 4)	22.6	(21, 5)	23.4	(21, 6)	22.8	(21, 7)	22.2				
(21, 0)	17.7	(21, 9)	21.9	(21,10)	22.5	(21,11)	22.9	(21,12)	23.8	(21,13)	25.8	(21,14)	25.8	(21,15)	23.8				
(22, 0)	22.3	(22, 1)	23.4	(22, 2)	22.5	(22, 3)	22.8	(22, 4)	20.8	(22, 5)	21.8	(22, 6)	19.8	(22, 7)	22.1				
(22, 0)	23.7	(22, 9)	22.4	(22,10)	23.2	(22,11)	22.3	(22,12)	21.5	(22,13)	21.8	(22,14)	21.8	(22,15)	21.8				
(23, 0)	22.8	(23, 1)	24.1	(23, 2)	24.8	(23, 3)	23.1	(23, 4)	23.2	(23, 5)	23.8	(23, 6)	24.3	(23, 7)	24.3				
(23, 0)	25.8	(23, 9)	25.2	(23,10)	25.2	(23,11)	27.1	(23,12)	25.7	(23,13)	27.6	(23,14)	23.8	(23,15)	24.7				
(24, 0)	25.7	(24, 1)	26.5	(24, 2)	24.8	(24, 3)	25.3	(24, 4)	25.2	(24, 5)	27.8	(24, 6)	24.4	(24, 7)	27.2				
(24, 0)	23.9	(24, 9)	24.3	(24,10)	25.7	(24,11)	24.9	(24,12)	24.4	(24,13)	23.9	(24,14)	23.9	(24,15)	22.8				
(25, 0)	27.3	(25, 1)	27.1	(25, 2)	27.2	(25, 3)	25.1	(25, 4)	26.9	(25, 5)	26.5	(25, 6)	26.5	(25, 7)	27.2				
(25, 0)	24.4	(25, 9)	24.9	(25,10)	23.9	(25,11)	25.8	(25,12)	25.3	(25,13)	25.2	(25,14)	26.8	(25,15)	25.3				
(26, 0)	21.5	(26, 1)	24.5	(26, 2)	24.5	(26, 3)	23.9	(26, 4)	23.2	(26, 5)	24.1	(26, 6)	24.5	(26, 7)	25.2				
(26, 0)	20.5	(26, 9)	20.7	(26,10)	19.9	(26,11)	21.9	(26,12)	21.7	(26,13)	21.9	(26,14)	22.6	(26,15)	23.9				
(27, 0)	27.3	(27, 1)	25.3	(27, 2)	27.5	(27, 3)	27.3	(27, 4)	25.5	(27, 5)	27.5	(27, 6)	22.5	(27, 7)	24.5				
(27, 0)	20.7	(27, 9)	22.3	(27,10)	21.9	(27,11)	23.7	(27,12)	23.8	(27,13)	23.1	(27,14)	21.3	(27,15)	23.4				
(28, 0)	23.1	(28, 1)	24.5	(28, 2)	23.5	(28, 3)	24.2	(28, 4)	24.4	(28, 5)	23.9	(28, 6)	25.6	(28, 7)	23.7				
(28, 0)	22.8	(28, 9)	21.5	(28,10)	22.3	(28,11)	20.9	(28,12)	20.3	(28,13)	22.4	(28,14)	21.1	(28,15)	23.2				
(29, 0)	26.9	(29, 1)	26.3	(29, 2)	27.8	(29, 3)	27.5	(29, 4)	25.6	(29, 5)	24.7	(29, 6)	27.8	(29, 7)	26.6				
(29, 0)	25.4	(29, 9)	25.1	(29,10)	24.4	(29,11)	24.4	(29,12)	26.4	(29,13)	25.9	(29,14)	24.5	(29,15)	25.6				
(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)	(,)				
(30, 0)	24.2	(30, 9)	22.0	(30,10)	22.7	(30,11)	21.4	(30,12)	22.3	(30,13)	25.5	(30,14)	24.6	(30,15)	24.1				
(31, 0)	21.7	(31, 1)	21.3	(31, 2)	19.4	(31, 3)	(,)	(31, 4)	21.8	(31, 5)	19.9	(31, 6)	20.9	(31, 7)	20.3				
(31, 0)	25.5	(31, 9)	27.1	(31,10)	25.5	(31,11)	(,)	(31,12)	23.3	(31,13)	24.3	(31,14)	23.4	(31,15)	22.4				
(32, 0)	27.3	(32, 1)	26.6	(32, 2)	25.8	(32, 3)	26.3	(32, 4)	25.6	(32, 5)	26.7	(32, 6)	25.2	(32, 7)	27.7				
(32, 0)	20.6	(32, 9)	21.5	(32,10)	22.4	(32,11)	21.7	(32,12)	21.7	(32,13)	20.7	(32,14)	23.9	(32,15)	21.3				
(33, 0)	21.5	(33, 1)	22.5	(33, 2)	22.7	(33, 3)	25.8	(33, 4)	25.3	(33, 5)	25.6	(33, 6)	22.9	(33, 7)	25.9				
(33, 0)	23.7	(33, 9)	23.4	(33,10)	23.2	(33,11)	23.6	(33,12)	24.8	(33,13)	24.6	(33,14)	21.3	(33,15)	23.3				
(34, 0)	20.8	(34, 1)	25.7	(34, 2)	25.6	(34, 3)	25.4	(34, 4)	23.8	(34, 5)	22.5	(34, 6)	22.4	(34, 7)	23.9				
(34, 0)	23.9	(34, 9)	23.7	(34,10)	23.3	(34,11)	22.2	(34,12)	22.5	(34,13)	20.6	(34,14)	25.6	(34,15)	26.4				

Table 3.1.1-1: RELATIVE PIXEL LUMINANCE MEASUREMENTS

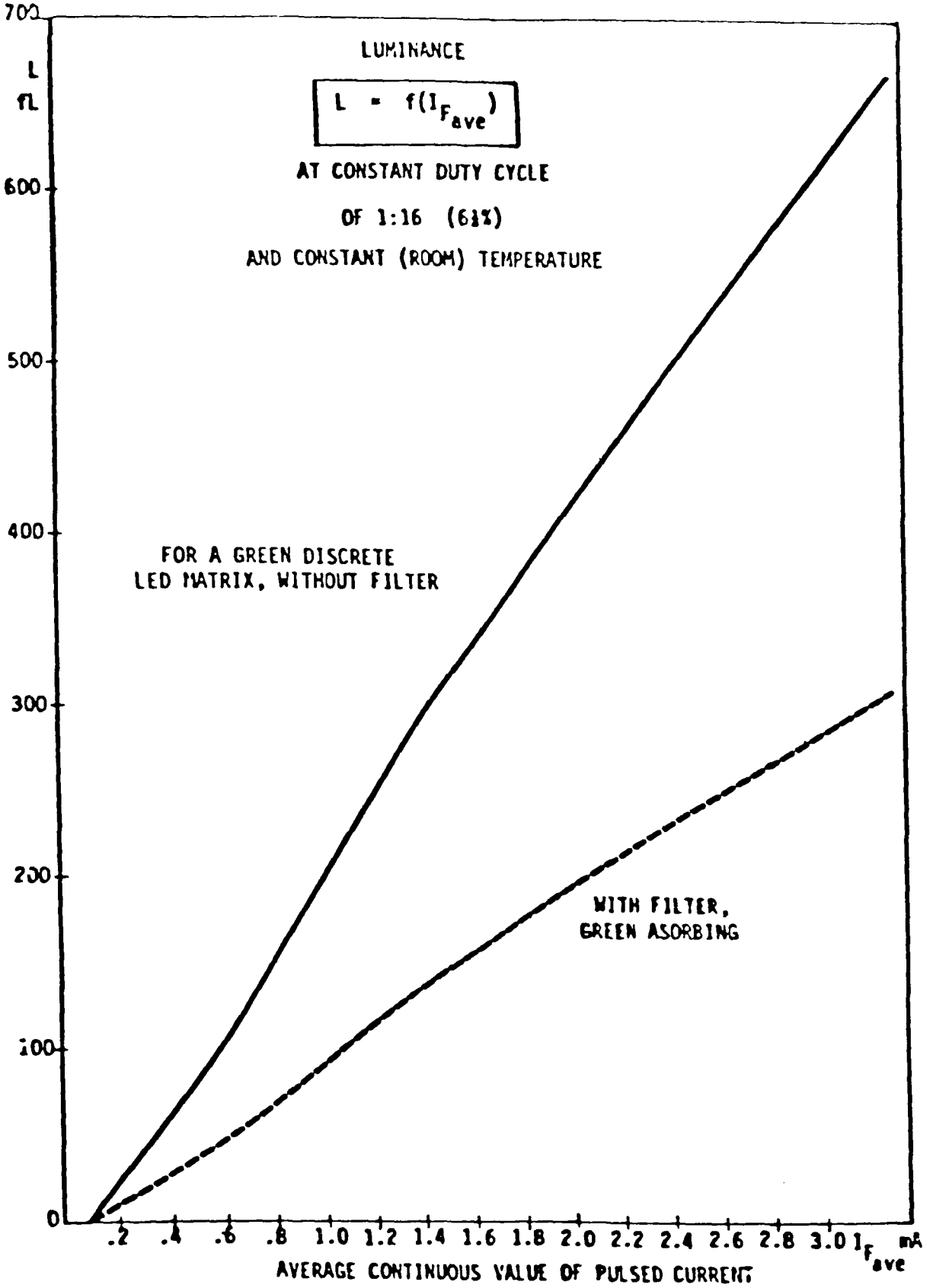


Figure 3.1.1-2: LED Luminance vs Drive Current

Veiling luminance was considered by measuring the ratio L_A/L_{DS} where L_{DS} is the off pixel luminance reflected from a standard black painted instrument bezel with approximately 4% diffuse reflectance. L_A was taken to be 4% of the ambient light level. Using a value for L_A of 80fL for $L_{ambient}$ at 2000fc (incident light at 45° to the surface) and the measured values of L_{DS} at 2000fc of 17.8 to 29.4fL, the value of LA/L_{DS} was calculated. Results showed values from 2.72 to 4.49. K_A (Reference 2-1) is approximately equal to 1 for values of $L_A/LDS < 6$. As a result, K_A (the adaptation/veiling luminance factor) was assumed to be 1.

Luminance control in the PPS/LRCU units is achieved by pulse width modulation of the LED drive circuitry. The resident firmware on the LRCU is currently capable of displaying 37 discrete luminance steps. The luminance steps are linear with a step size of 0.17% in duty cycle or a luminance change of 2.7 fL per step. Figure 3.1.1-3 shows the relation between duty cycle and the average display brightness. The maximum duty cycle is 6.25% as a consequence of the 16 row multiplexing of the LED matrix.

Verification of the appropriate range of luminance control was accomplished by measuring the luminance range of the displays at 0° over a range of ambient illumination. A photometer, sungun and reflectance standard were oriented as shown in Figures 3.1.1-4a,c to determine levels of ambient illumination. The reflectance standard RS-1 is replaced by the display in performing the luminance control measurements. The photometer is adjusted to measure a circular field of 0.016" and one of the six "average" pixels on the display is used in the measurements. The measurements of the pixel luminance are then compared with the appropriate control law curves as shown in Figure 3.1.1-5 to verify that the maximum and minimum values of perceived luminance, ΔL_p lie within the limits of those curves as a function of ambient illumination. Figure 3.1.1-4b shows the orientation of ambient source, display and photometer for the viewing angle measurements (see Section 3.1-4) and contrast ratio measurements at non-zero viewing angles. This photometer may be moved in the X-Y plane.

3.1.2 Contrast Ratio

The display contrast ratio was determined by measuring ΔLp and L_{DA} (defined below) for an average pixel as a function of ambient light (10^{-6} - 10^{4} fc). The displays

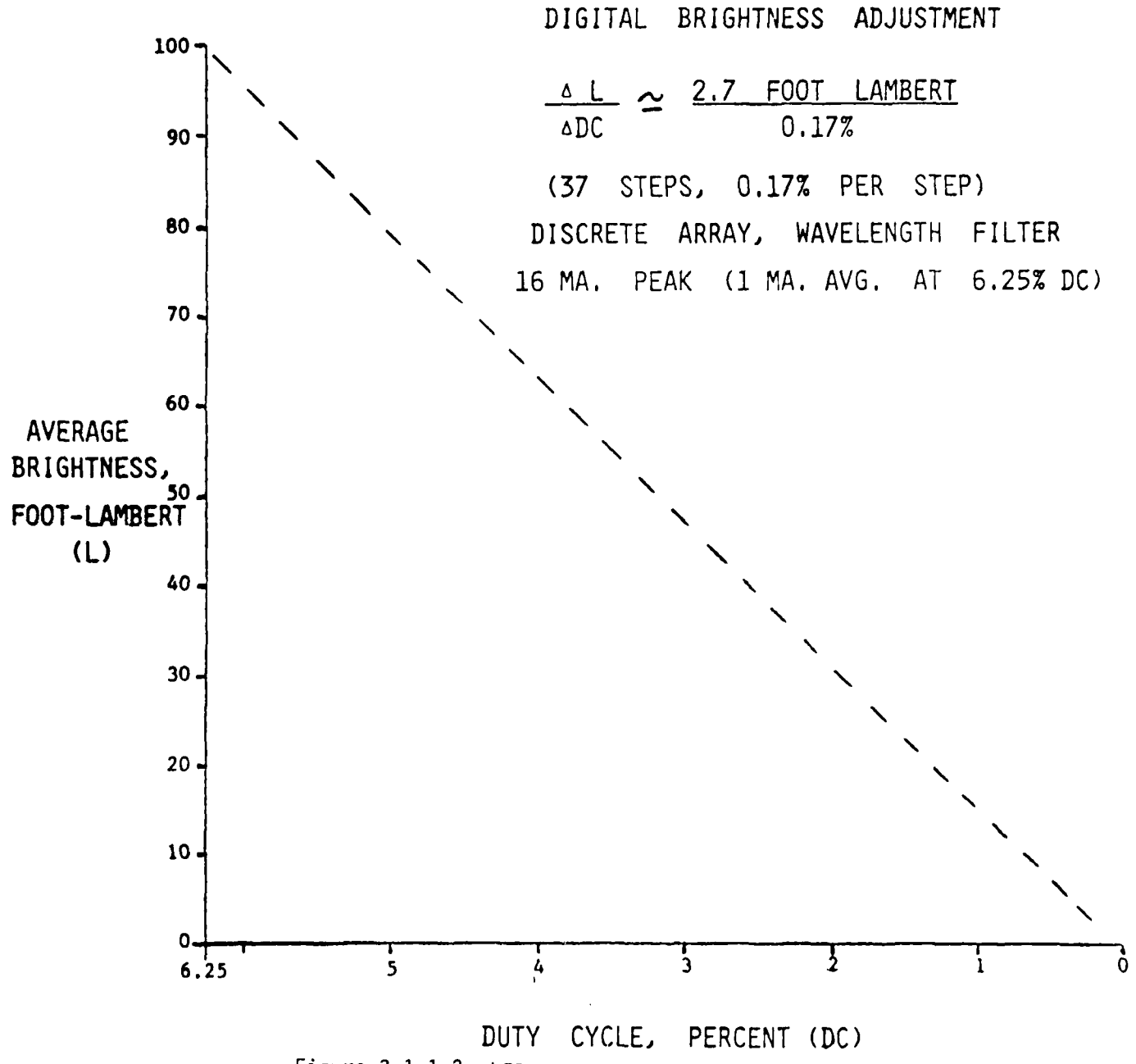


Figure 3.1.1-3: LED LUMINANCE CONTROL RELATION

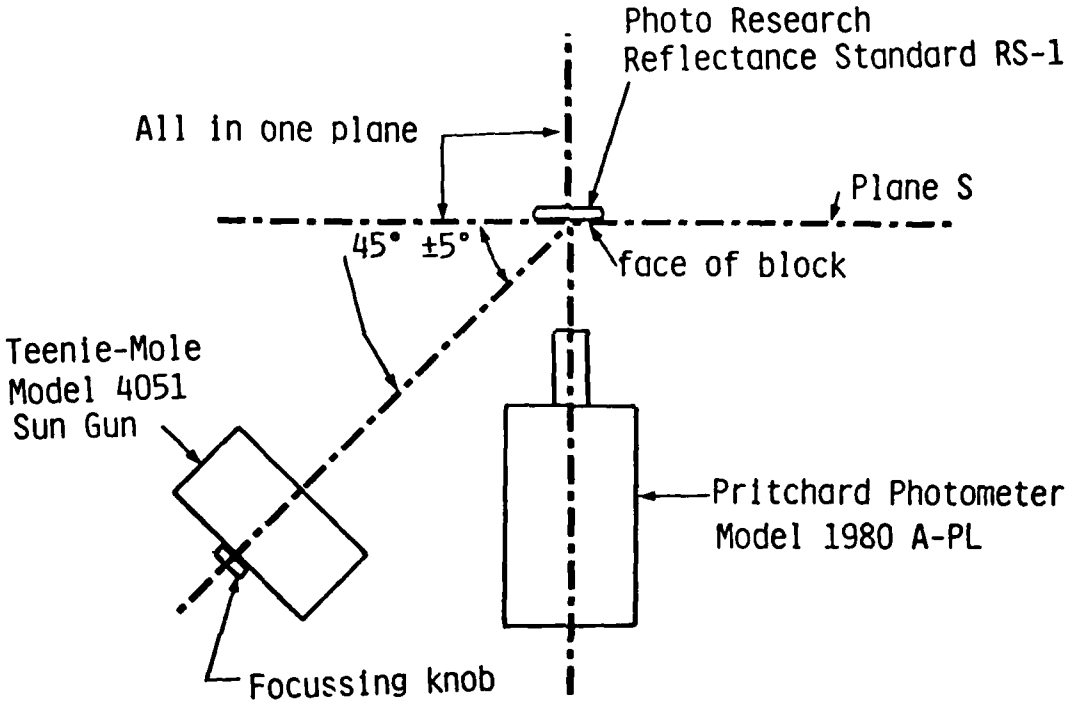


Figure 3.1.1-4a:
LUMINANCE CONTROL VERIFICATION TEST FIXTURE SCHEMATIC

CONTRAST MEASUREMENT SET-UP FOR 45° VIEWING ANGLE

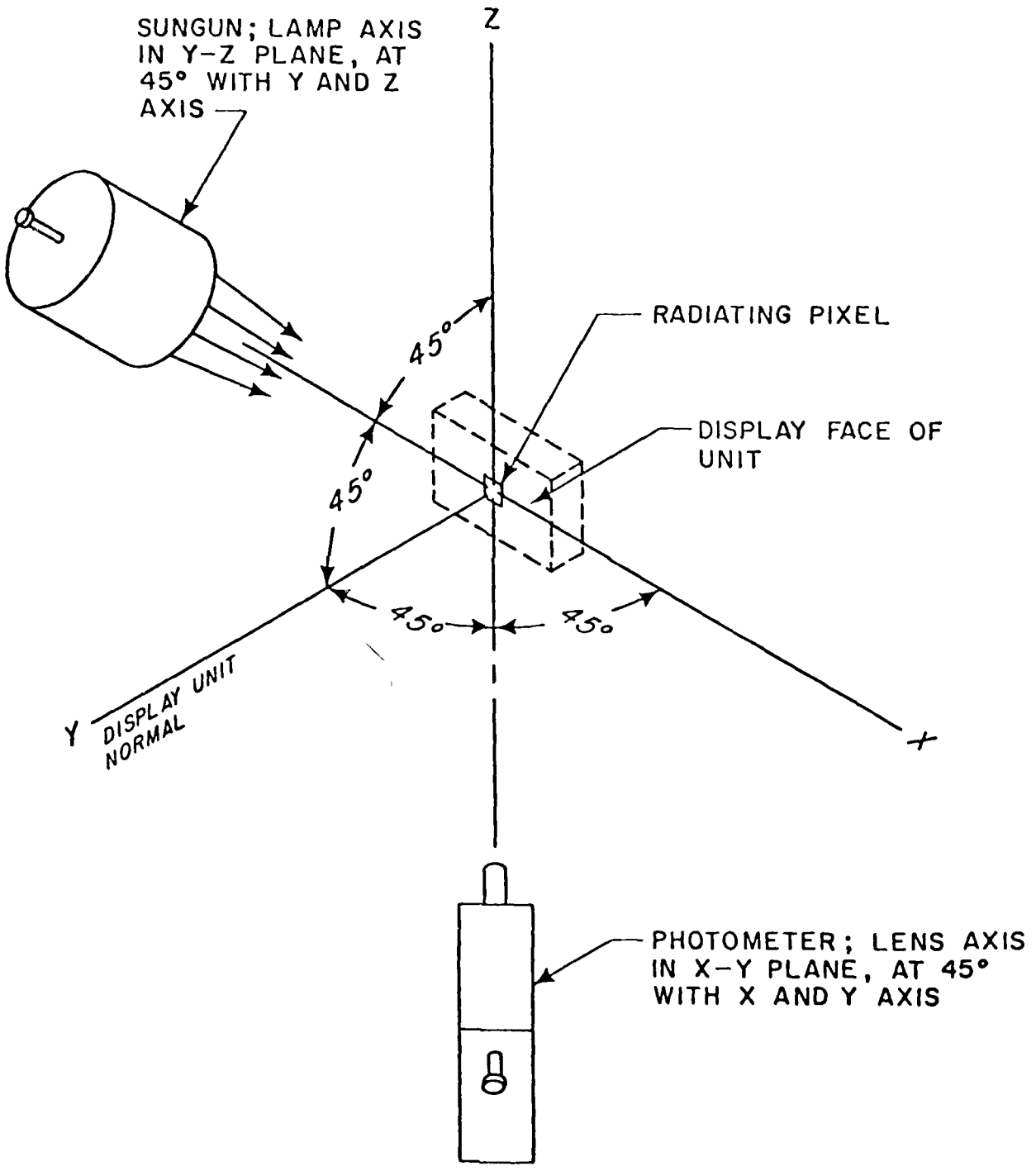


Figure 3.1.1-4b:
CONTRAST RATIO vs VIEWING ANGLE TEST FIXTURE SCHEMATIC

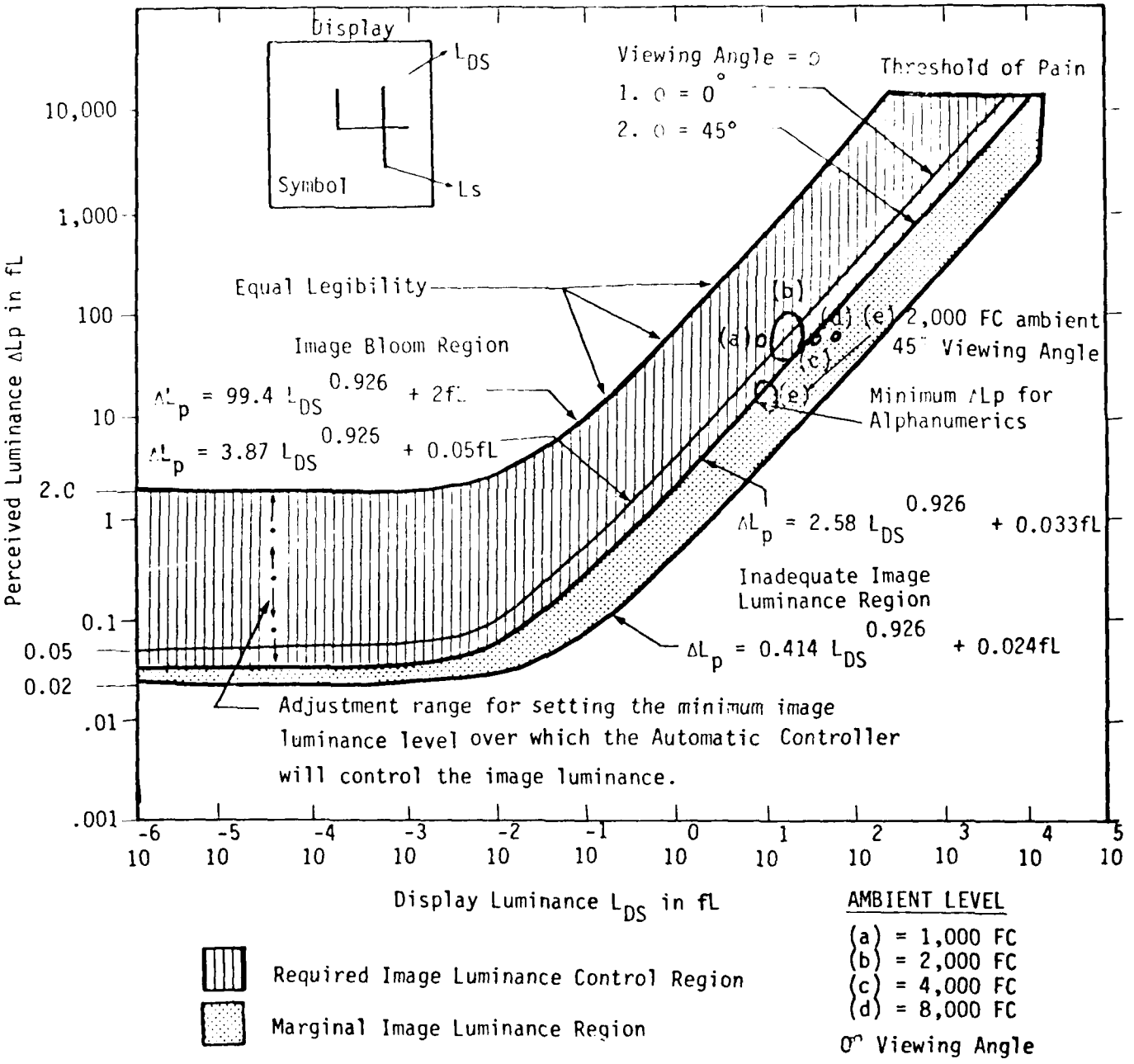


Figure 3.1.1-5 : PERCEIVED LUMINANCE CONTROL REQUIREMENTS

are provided with a mask with apertures over the pixel centers. Since the mask area is more than three times as large as the pixel aperture area, the mask is considered the dominant background for on pixels. At this time, sunlight readability requires a diffuse front surface. This layer is located approximately 1/8 inch in front of the aperture mask and pixels position, five times the center to center spacing of the radiant sources or off-pixels. Sunlight reflected by the rear structure to the observer has traveled twice through this partial scattering layer. As a result of this scattering, it is no longer possible to obtain "pure" L_{DS} and L_{DB} readings. Any reading, when aimed at the center of an off-pixel (L_{DS}) will unavoidably contain some reflections. The best measure of contrast therefore is, to compare the center of on-pixel luminance, L_S, with the area-averaged display background luminance, which for now we will call L_{DA}. Using the earlier concept of contrast definition, we will use $CR = (L_S - L_{DA})/L_{DA}$. The majority of measurements were taken at 0^o viewing angle. Limited measurements were also taken at 45^o to establish the display viewing angle. Figure 3.1.2-1a shows the contrast ratio as a function of ambient light for a matrix of discrete LED's measured at 0^o viewing angle and including filtering over the display.

Figure 3.1.2-1b shows a contrast ratio comparison between the discrete and monolithic LED matrices. The monolithic matrix performance exceeds that of the discrete matrix by a factor of approximately 3. Figure 3.1.2-1c shows the contrast ratio and perceived luminance as a function of viewing angle for the on-pixel luminance vs. mask off-pixel average luminance L_{DA}. These measurements were made at a 2000fc ambient light level. Table 3.1.2-1 shows sample specific values measured for L_{DS}, L_{DB}, and L_{DA} in forming the contrast ratios. Perceived luminance values at 0^o and 45^o are also plotted as data points in Figure 3.1.1-5. For 2000fc ambient light levels, more samples were examined and the data cover a region in the diagram.

3.1.3 Color

Display color was determined by measuring the spectral emission of the LED's using a monochromator and the Pritchard photometer (see Figure 3.1.3-1). The dominant wavelength was determined and compared with the desired range of 550-575 nm. Color uniformity was hard to measure on a pixel by pixel basis because of the low signal to noise ratio per pixel in the narrow wavelength band (10 nm) sampled by the monochrometer. An alternative approach for measuring color uniformity was devised.

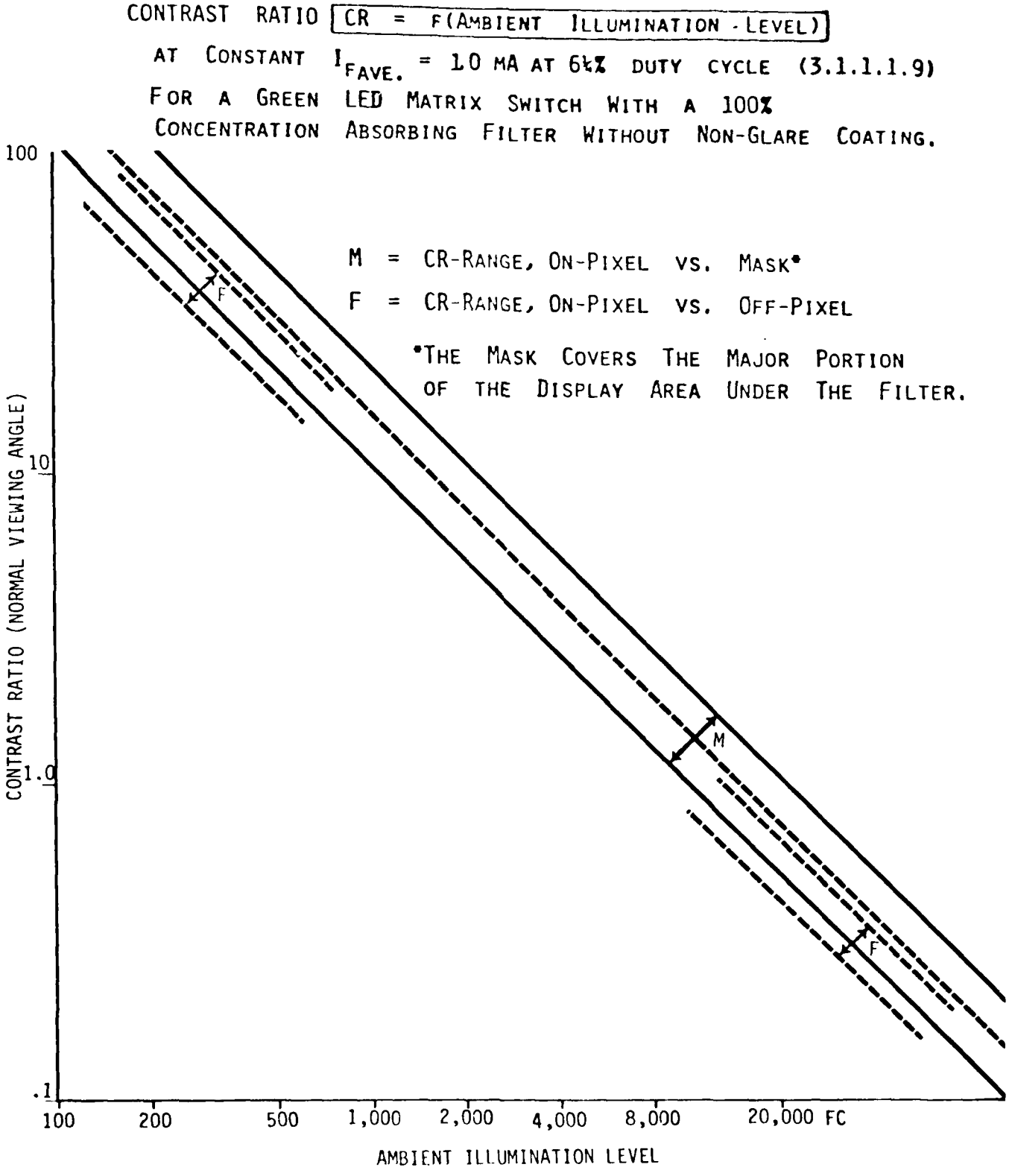


Figure 3.1.2-1a: CONTRAST RATIO VS. AMBIENT ILLUMINATION

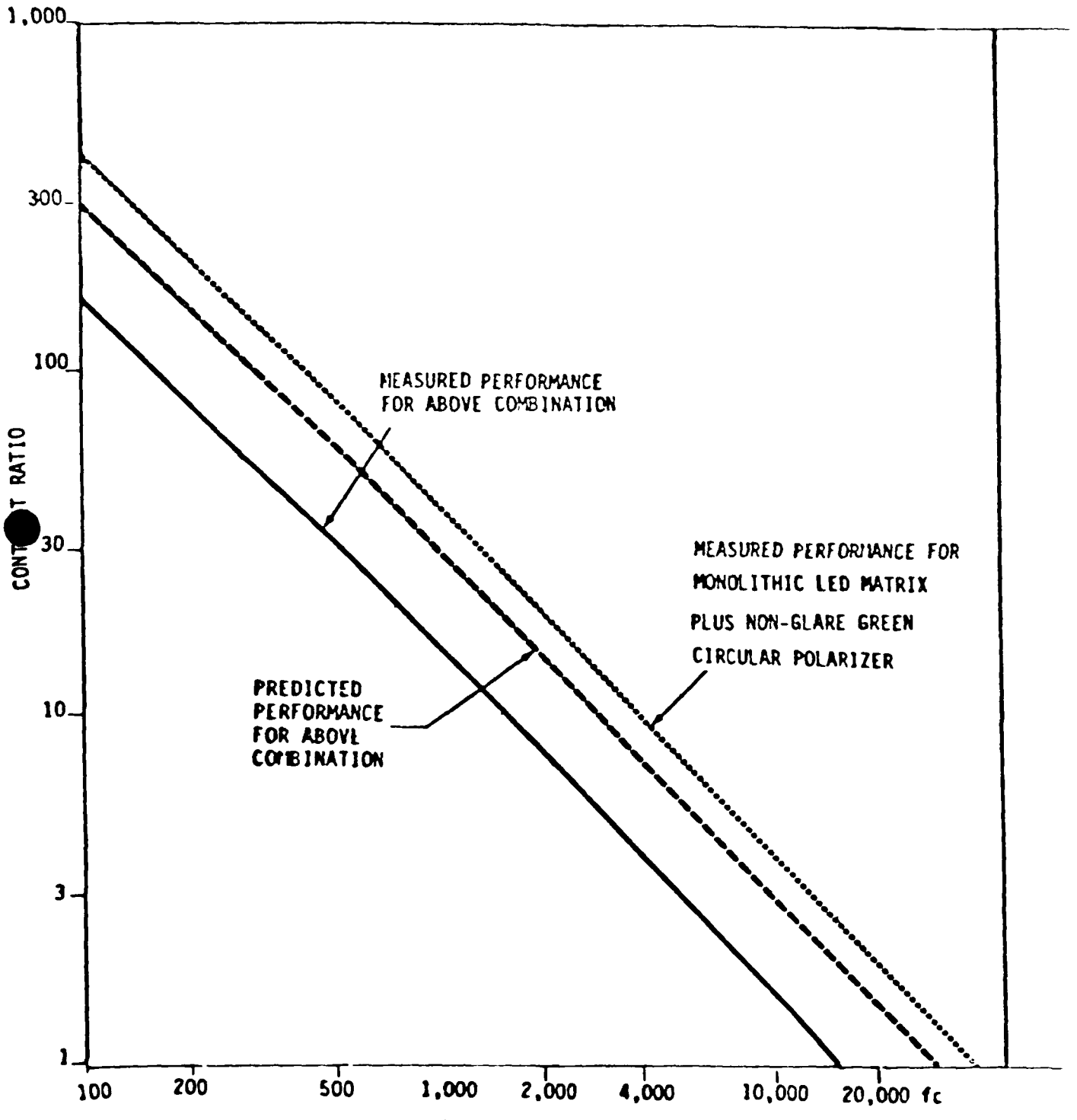


Figure 3.1.2-1b: CONTRAST RATIO COMPARISON BETWEEN DISCRETE AND MONOLITHIC LED ARRAYS

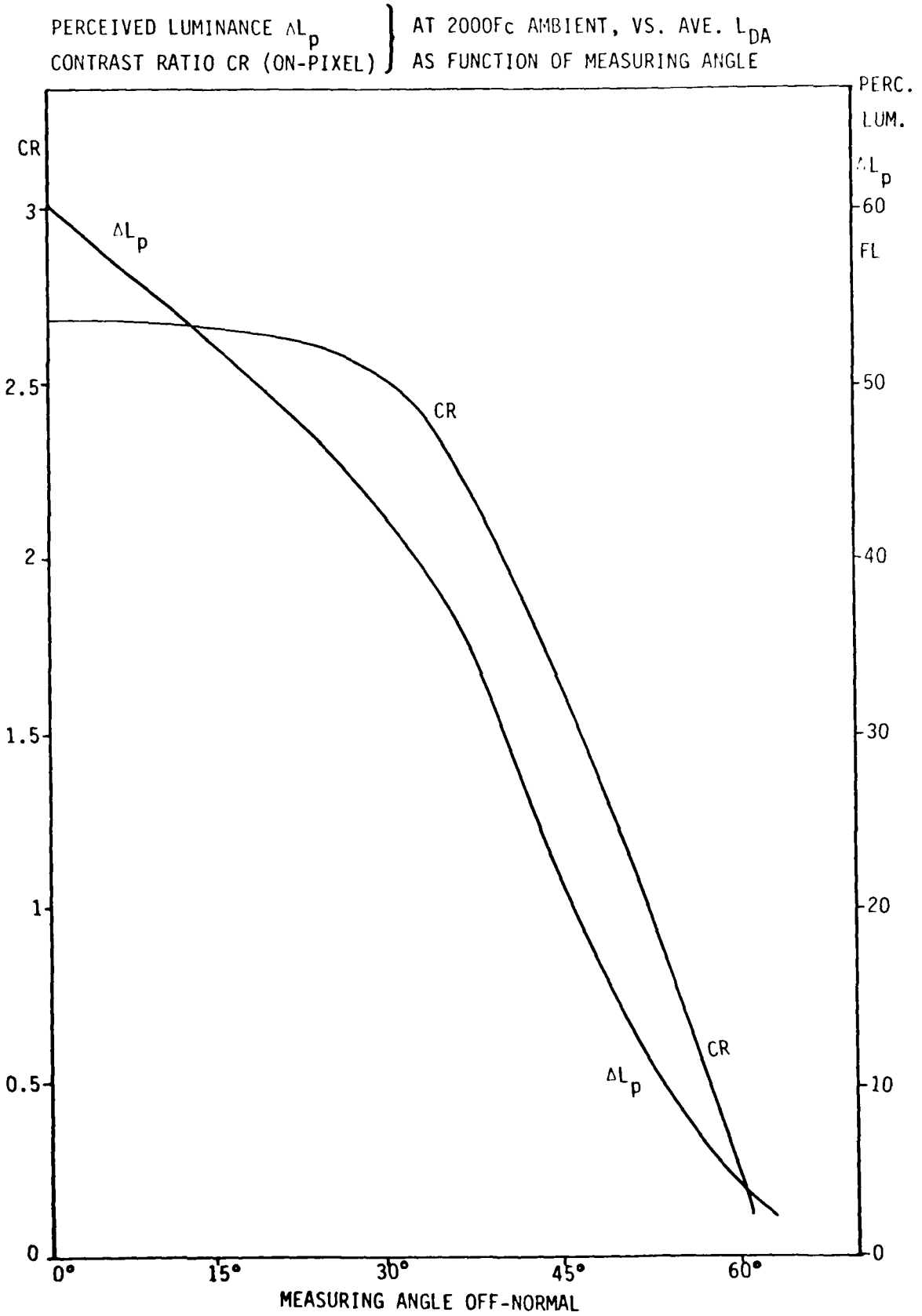
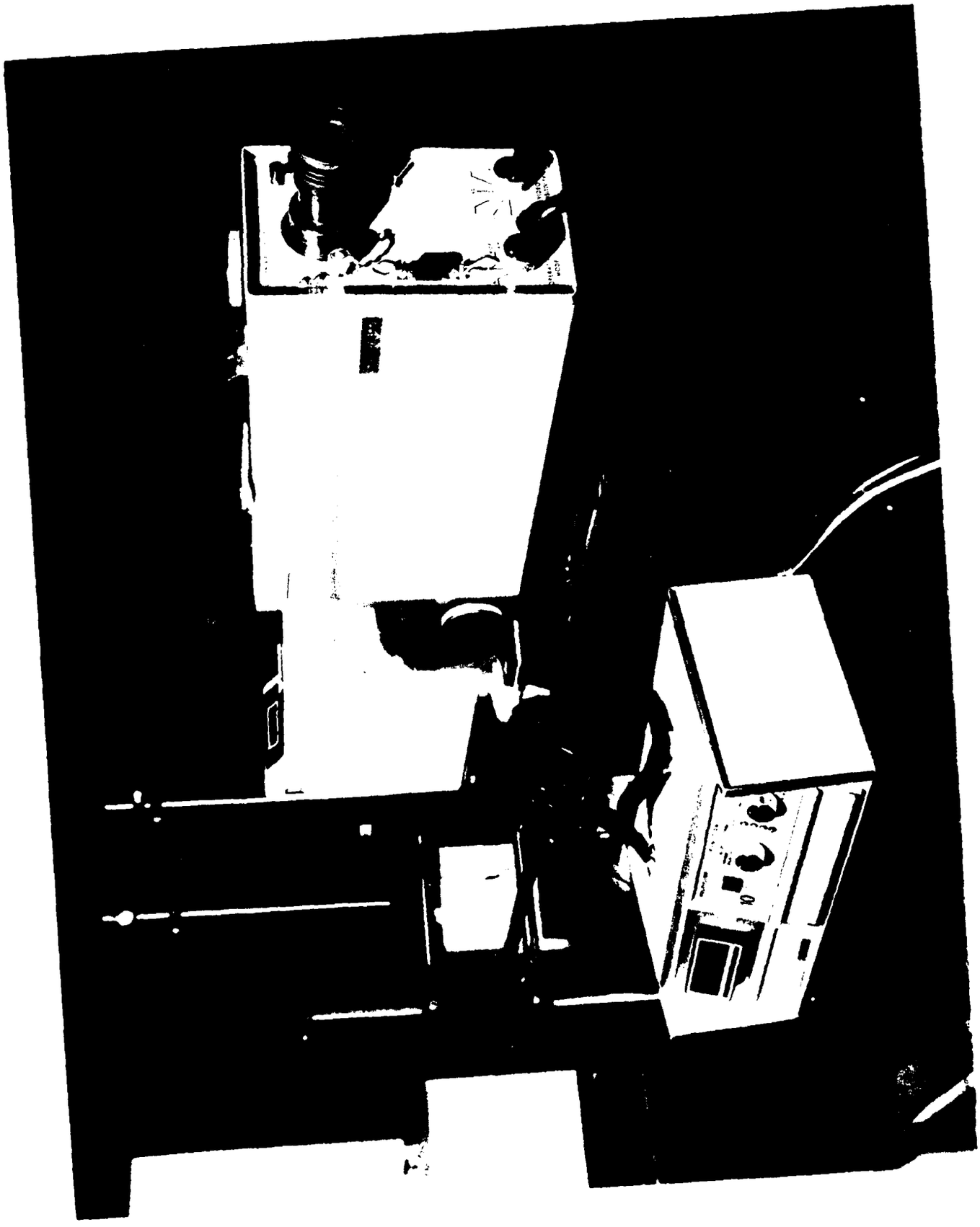


Figure 3.1.2-1c CONTRAST RATIO VS. VIEWING ANGLE



Quantity at 2,000 fc:	Range	Average
L_{DS}	16.5 - 24.1 fL	19.9
L_{DB}	12.7 - 20.05fL	16.5
L_{DA}	13.0 - 19.8fL	16.2

Ambient, fc:	1000	2000	4000	8000
$L_s - L_{DA}$:	55.7	56.4	57.2	62.6
L_{DA}:	8.3	16.1	36.5	68.0
$CR = (L_s - L_{DA})/L_{DA}$:	6.68	3.50	1.7	0.921

Table 3.1.2-1: Contrast Ratio Measurement Data
(80% Concentration filter, normal viewing angle)

In this technique the display module is placed under a photographic camera such as the Polaroid MP-4 (see Figure 3.1.3-2). In otherwise total darkness, all the pixels are driven, one at a time, at the same current and pulse duration, with the camera "open." A color picture is made in which each individual pixel can be clearly seen. This color picture is reviewed and when the unaided eye cannot observe different colors between pixels, the color uniformity within a module is acceptable. The mean or peak wavelength λ_p for each individual pixel (λp_p) should now fall well within a ± 5 nm range from the mean dominant wavelength of the module (λp_m).

3.1.4 Viewing Angle

The viewing angle range for the PPS units is defined by contrast ratio measurements as a function of angle.

3.1.5 Crosstalk

Crosstalk between different LED"s in the dot matrix array may result from optical or electrical excitation. When an individual pixel is driven, in the case of optical

crosstalk, some of its emitted radiation may be received by adjacent "off" pixels. These adjacent pixels may then appear to have some low brightness luminance.

When an optical filter covers the display, especially when that filter includes a scattering layer such as a non-glare coating, some of the emission of the "on" pixel may strike the filter at such angles that adjacent pixels appear to have some radiation. What the observer (or measuring instrument) notices in this case is a combination of the two effects. On a completed switch, only the combined effect can be measured.

Pixel optical crosstalk is defined as $OC_P = L_{DS_n}/L_{s_o}$, where L_{s_o} is the on-pixel luminance at zero ambient illumination level, and L_{DS_n} is the off-pixel luminance of a pixel that is n places removed from the driven pixel.

For these measurements, driven pixels had a luminance L_P that was close to the matrix average. A single pixel was driven with the standard $I_{Fave.}$, and the pixel L_{s_o} was measured. While the pixel remained "on", the photometer was aimed at adjacent pixel centers, horizontally on both sides of the driven pixel (along the same row), and vertically both "above" and "below" the driven pixel (along the same column). The luminance L_{DS_n} of each adjacent pixel was recorded by horizontal or vertical position removed from the driven pixel.

These measurement sets were made successively for two driven pixels each of three different display units. The driven pixels were chosen also so that there are at least five adjacent pixels on all four sides of the driven pixels, and the two driven (at different times) pixels of one dfisplay unit should not share a row or a column. If there was a structure discontinuity in the matrix display unit, that would cause a certain adjacent pixel to show less parasite luminance than its "associated" pixel on the opposite side of the driven pixel, then only the readings of the higher luminance pixel of these two were used for this evaluation.

The five most adjacent pixels on all four sides of each driven pixel were measured. The average of all valid readings (per above paragraph) for each H_n and each V_n

position were established for the three display units. From these averages, the ratio OC_P was determined and plotted as shown in Figure 3.1.5-1a,b.

Figure 3.1.5-1a shows the results for an unfiltered discrete LED matrix. The nominal allowable upper limit for OC_P was set at 5%. This value is indicated on the figure. Note that the limit is satisfied in both the vertical and horizontal directions. Figure 3.1.5-1b shows the same results for a filtered display. In this case, the maximum value of OC_P one position removed is 5% for positions in the vertical direction. The filter thus increases the optical crosstalk. Electrical crosstalk was required to fulfill the relation Lec 0.02 L_p. In general electrical crosstalk was anticipated at random locations on the matrix array as opposed to LED's adjacent to an excited LED. The electrical crosstalk was measured subjectively by inspecting the LED arrays for extraneous diode illumination when characters or patterns were displayed. The only observance of electrical crosstalk occurred at the lowest step of luminance control in which the row of LED's immediately below the excited row also showed illumination. This problem has been traced to timing problems in the drive circuitry during the lowest duty cycle level.

3.1.6 Flickering and Stroboscopic Effects

The presence of flickering and or stroboscopic effects was evaluated subjectively by observation of the operating displays. The refresh rate of the displays was set at 500 Hz to avoid flicker and stroboscopic problems and observations of switch operation to date show no evidence of flicker during steady state operation. The observations of flickering have been carried out using four subjects and from one to twenty switches in close proximity, and ambient lighting from room darkness to approximately 5000 ft-C. Both graphic and alphanumeric formats were used. Switch luminance settings from 2 to 100 fL were used. The presence of stroboscopic effects requires testing of the displays under vibration. This was done under the vibration testing of Section 3.3.3. No stroboscopic effects were seen in lighting conditions from room ambient light to darkness.

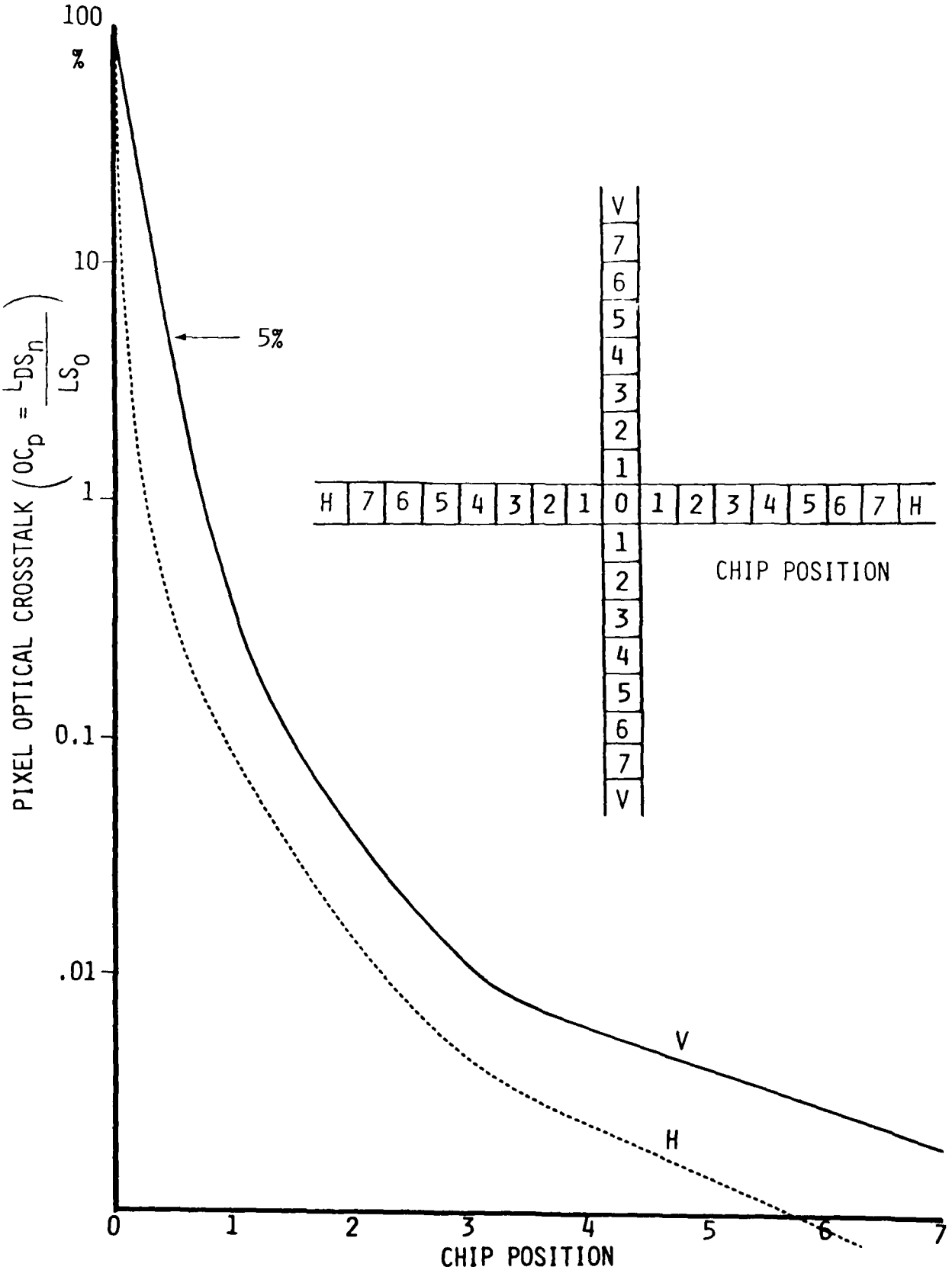


Figure 3.1.5-1a: OPTICAL CROSSTALK FOR UNFILTERED DISPLAY

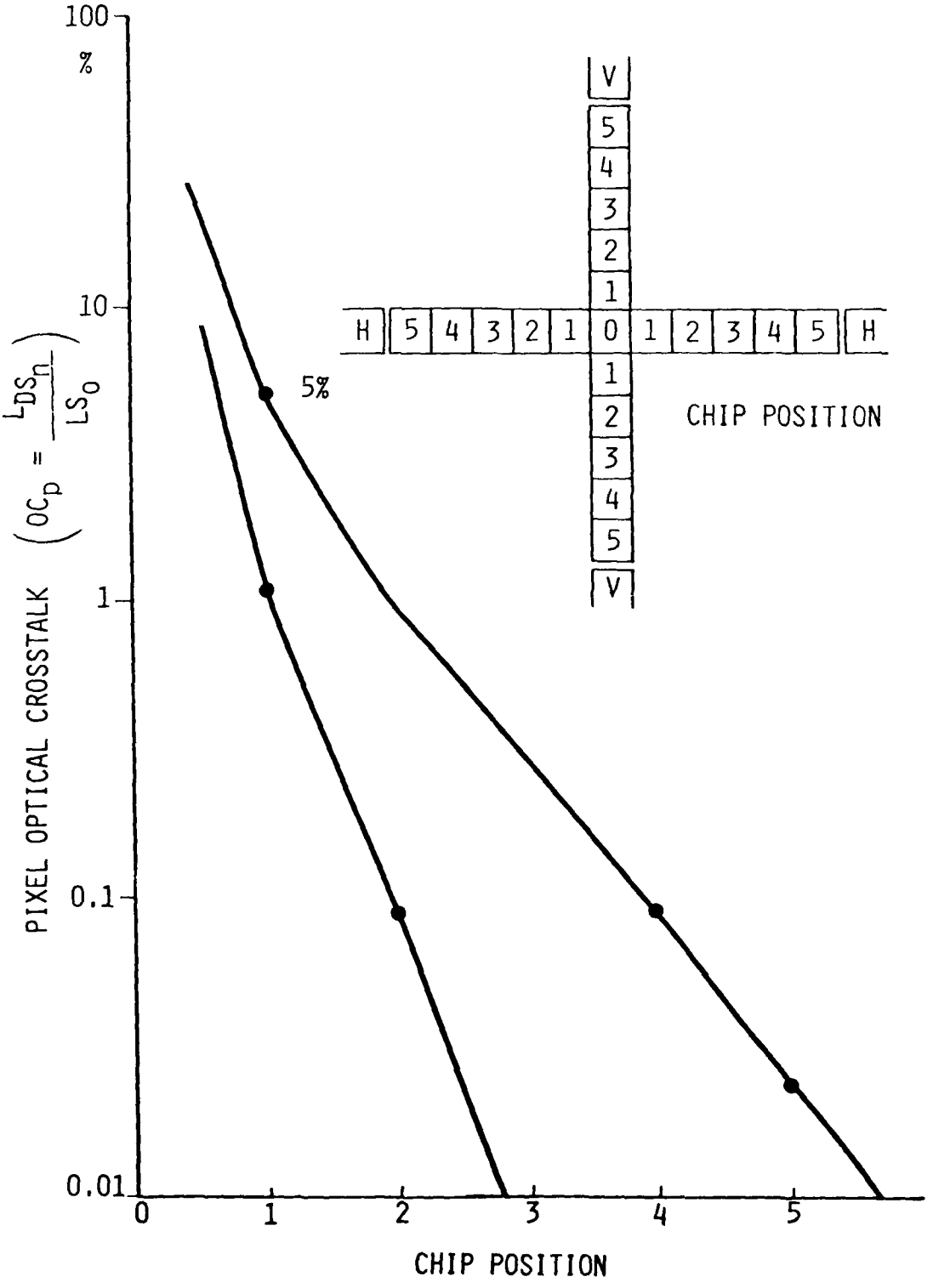


Figure 3.1.5-1b: OPTICAL CROSSTALK FOR FILTERED DISPLAY

3.1.7 Effect of Filters and Fingerprints

A contrast enhancement filter was used over the display to provide improved optical characteristics and to serve as a touch activation surface. To limit the number of optical interfaces (for improved perceived luminance and contrast) it was decided to use the minimum number of components. Therefore, the contrast enhancement filter had to function also as the pushable front element. This ruled out glass, and we were limited to a plastic. Circular polarizers were tried for engineering purposes but could not be obtained in the required thickness tolerances, nor in molded form. For production units, therefore, the choice was non-polarizing bandpass filters which we could mold in our own facilities, at the required thickness tolerances. We expect to improve upon this bandpass filter after a further material search. For the anti-glare treatment we chose a commercially available display coating service which provides an outer surface treatment with both scratch resistance and anti-glare properties. This surface treatment is probably also not the final choice; we are in the process of developing this capability, with consistent results, in our own facilities. Further information will be made available when specific changes have been decided upon. Transmission characteristics of the filter in current use are compared with the LED emission characteristics in Figure 3.1.7-1a. Figure 3.1.7-1b illustrates the structure of the contrast enhancement filter assembly.

The effect of fingerprints on the display was also evaluated subjectively. A light matte finish was applied to the display filters to reduce the effect of fingerprints. For a viewing angle normal to the display, the fingerprint was faintly visible but did not appear to affect the display image quality significantly. Observations were made with the switch displays showing a variety of alphanumeric character formats. The most noticeable effect occurred when the display viewing angle was such that specular reflections from the ambient light (approximately 80-10,000fc) occurred. In this case the fingerprints changed the reflection characteristics considerably and were highly visible. Under these conditions the glare from the matte finish was actually reduced by the fingerprint film, thus improving visibility.

3.1.8 Set and Font Size

The font sizes for the PPS units were fixed by the matrix resolution, however the rendition of the fonts are variable to some degree. This study considered only

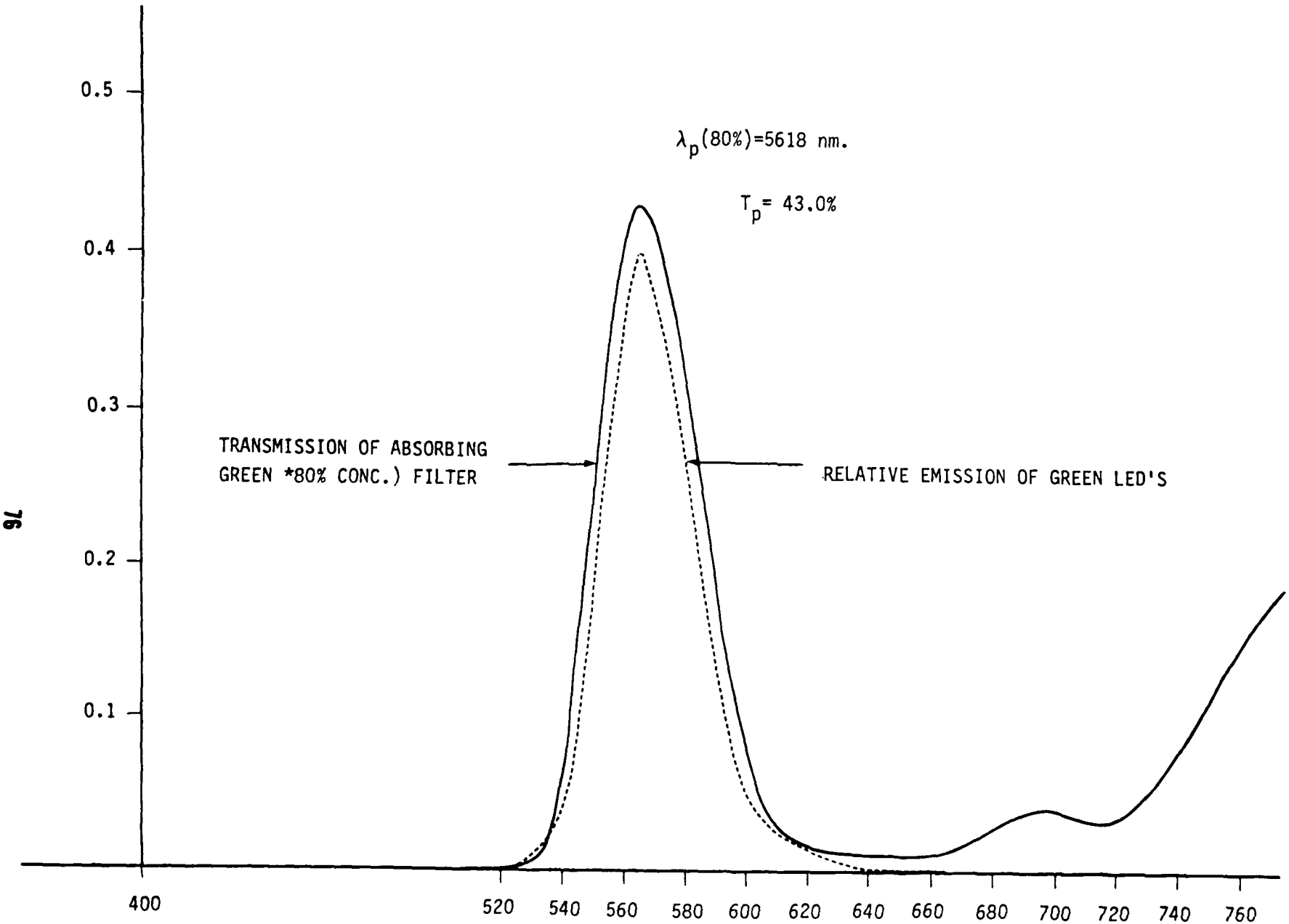


Figure 3.1.7-1a: CONTRAST ENHANCEMENT FILTER TRANSMISSION CHARACTERISTICS

CONTRAST ENHANCEMENT STRUCTURE

Scale: 50:1 Approximate dimensions in inches.

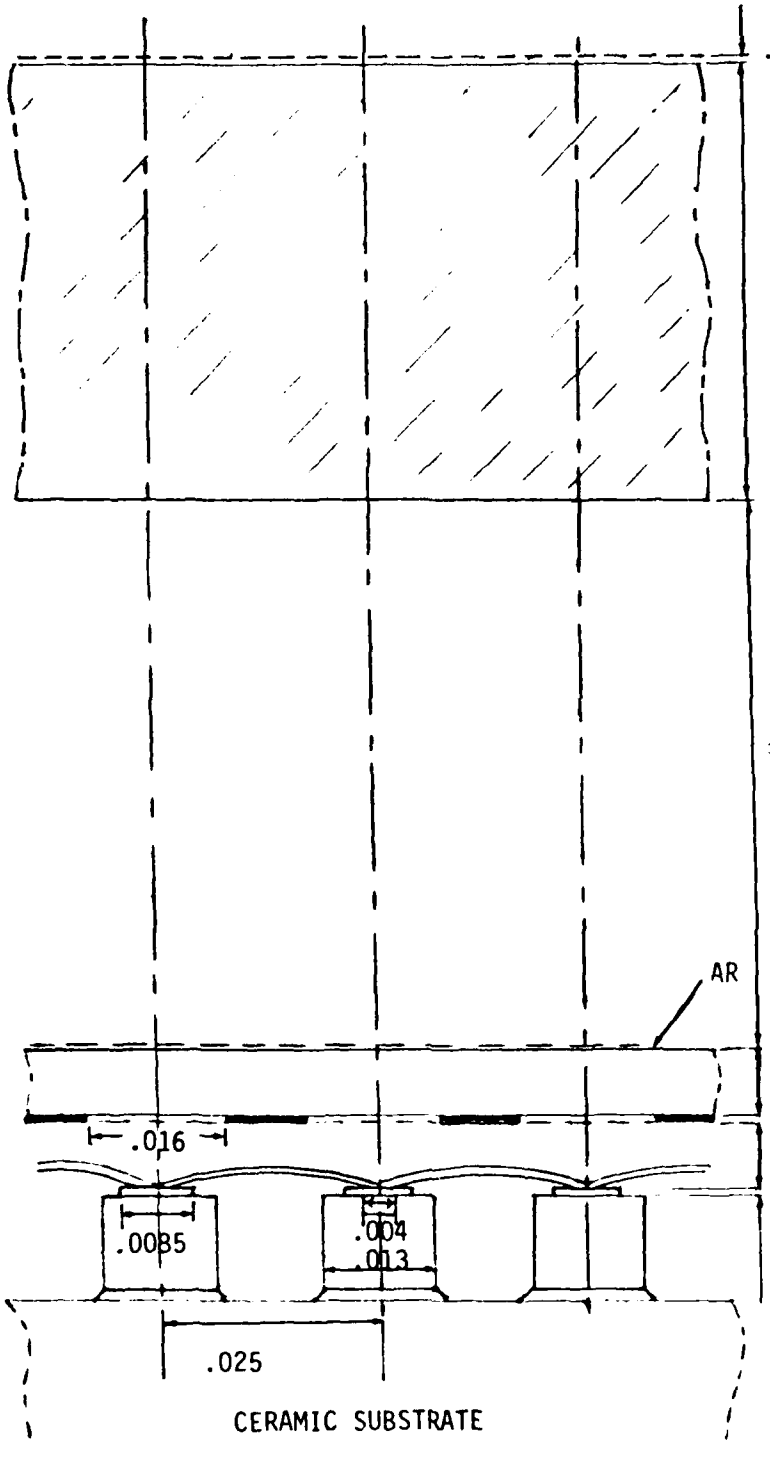


Figure 3.1.7-1b: CONTRAST ENHANCEMENT FILTER STRUCTURE

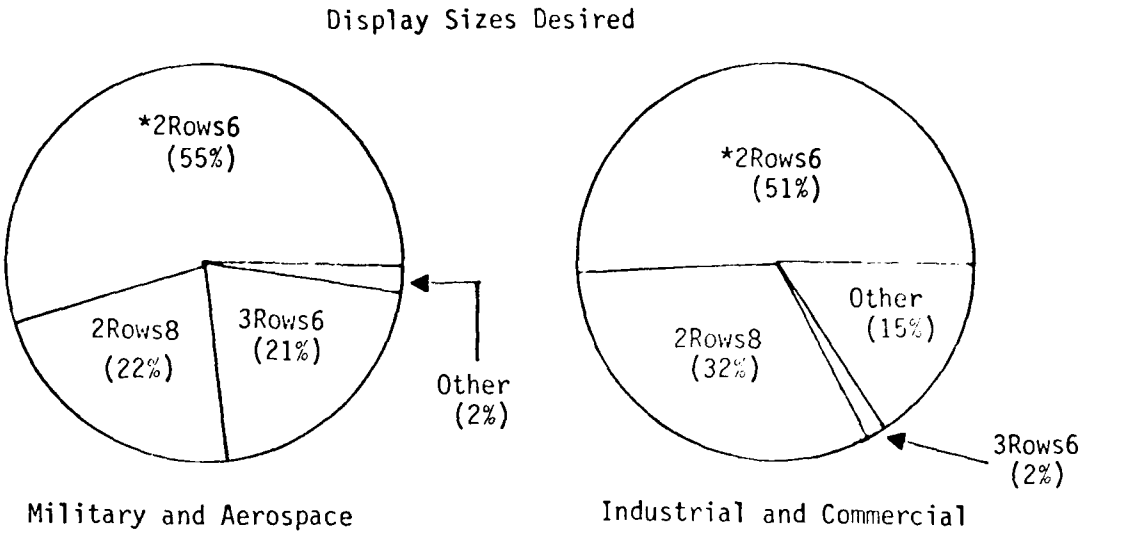
uppercase letters, numerals and a few symbols, where a 5 x 7 font is adequate for a dot matrix portrayal (Reference 3-1).

A survey was made of potential users of the PPS to determine probable requirements for the number of characters and rows required for legends. The choice of 2 rows of six characters, when applied to a full dot matrix speaks to the majority of the users. Military, commercial and industrial users were surveyed on the questions of number of rows, number of characters and interface technique. The prototype configuration was sized for 2 rows of 6 characters while full scale production most certainly would expand to other forms including mixing colors within a single display. Figure 3.1.8-1 shows the relative size configurations with respect to the number of characters as well as the desired interface modes as related to display desires. Figure 3.1.8-1 (a),(b) shows the number of rows and characters desired by potential users. Figure 3.1.8-1(c) shows the interface modes proposed and their relative preferences. Mode A involves the transfer of 1 character at a time to the switch LRCU. Mode B utilizes stored messages in the LRCU memory. Mode C transfers pixels or groups of pixels to the LRCU from the MFK controller. This mode is used for the display of graphic information.

The character size chosen is adequate for a 26"-28" viewing distance although some improvement in legibility would be obtained with a larger character size (Reference 3-2). The use of a larger font 10 x 14 for the display of digits used for data entry would also be an advantage. The PPS 5 x 7 font was evaluated and a number of minor changes were suggested. The recommended rendition is shown in Figure 3.1.8-2. Most of the changes are designed to prevent confusion in the event of a row or column failure or to reduce the number of LED's being lit as a power saving measure. At this time, power and display costs form the principal barriers to the use of a four LED pixel as suggested in Reference 3-3.

3.1.9 Display Formats

The PPS/LRCU units were tested for display of alphanumeric characters and bit map graphic patterns. Both display formats worked with no problems, thus verifying the software command structure associated with display formation.



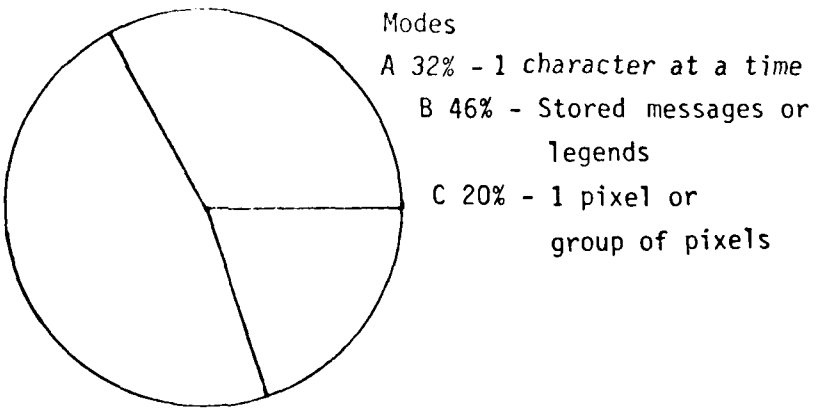


Figure 3.1.8-1: DESIRED DISPLAY FORMATS AND INTERFACES

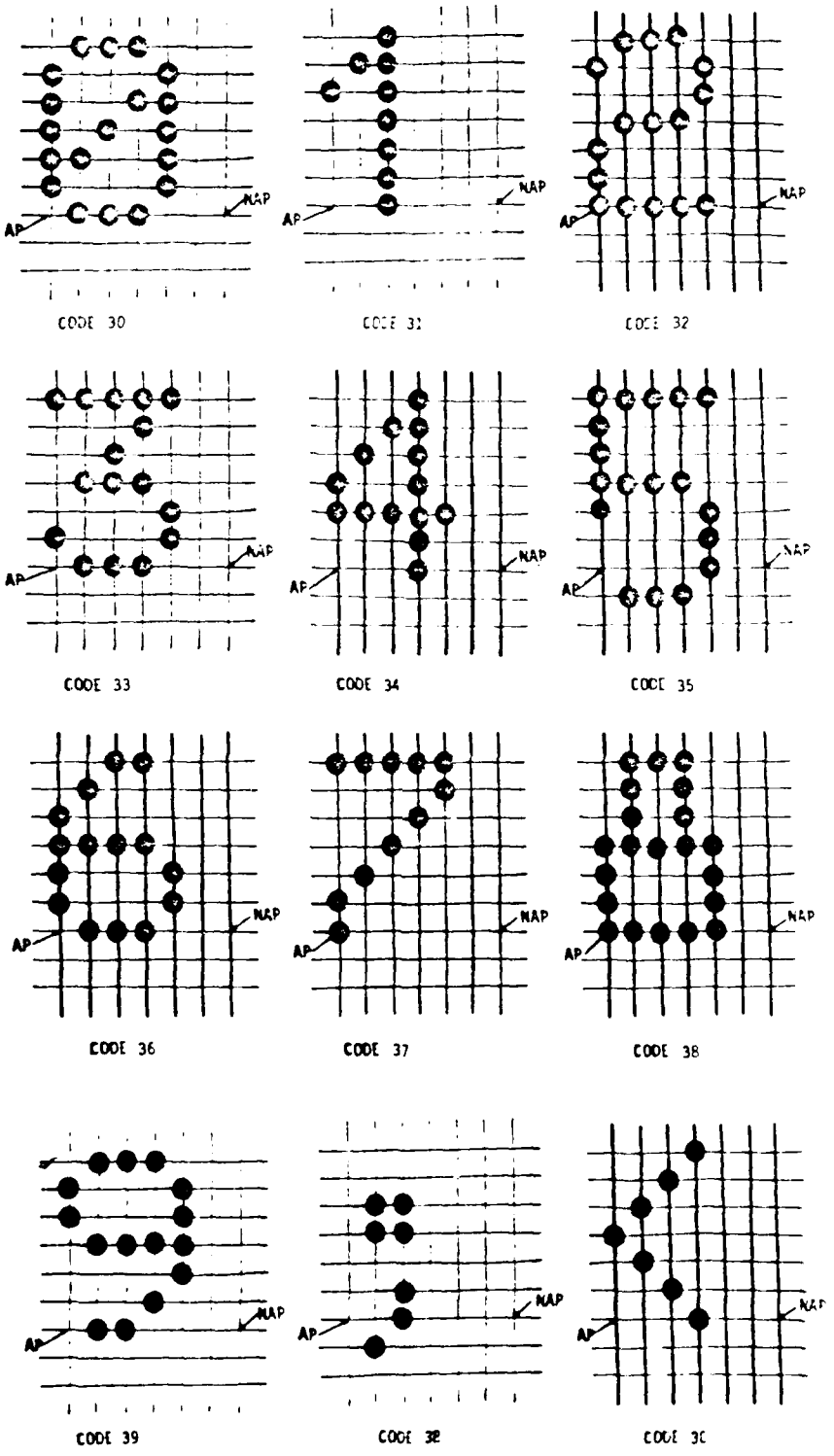


Figure 3.1.8-2: CHARACTER AND SYMBOL FORMATS

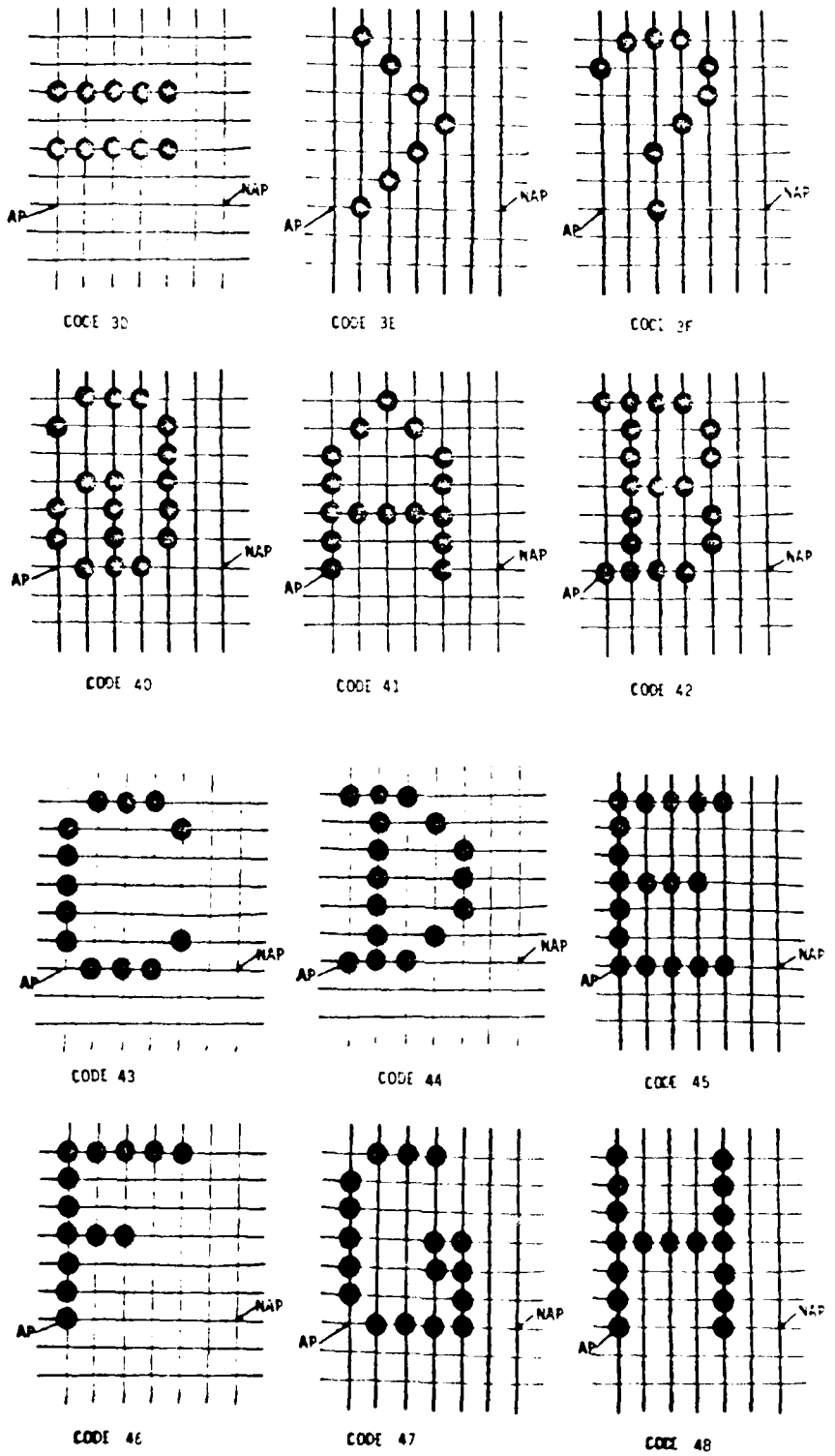


Figure 3.1.8-2: CHARACTER AND SYMBOL FORMATS (CONTINUED)

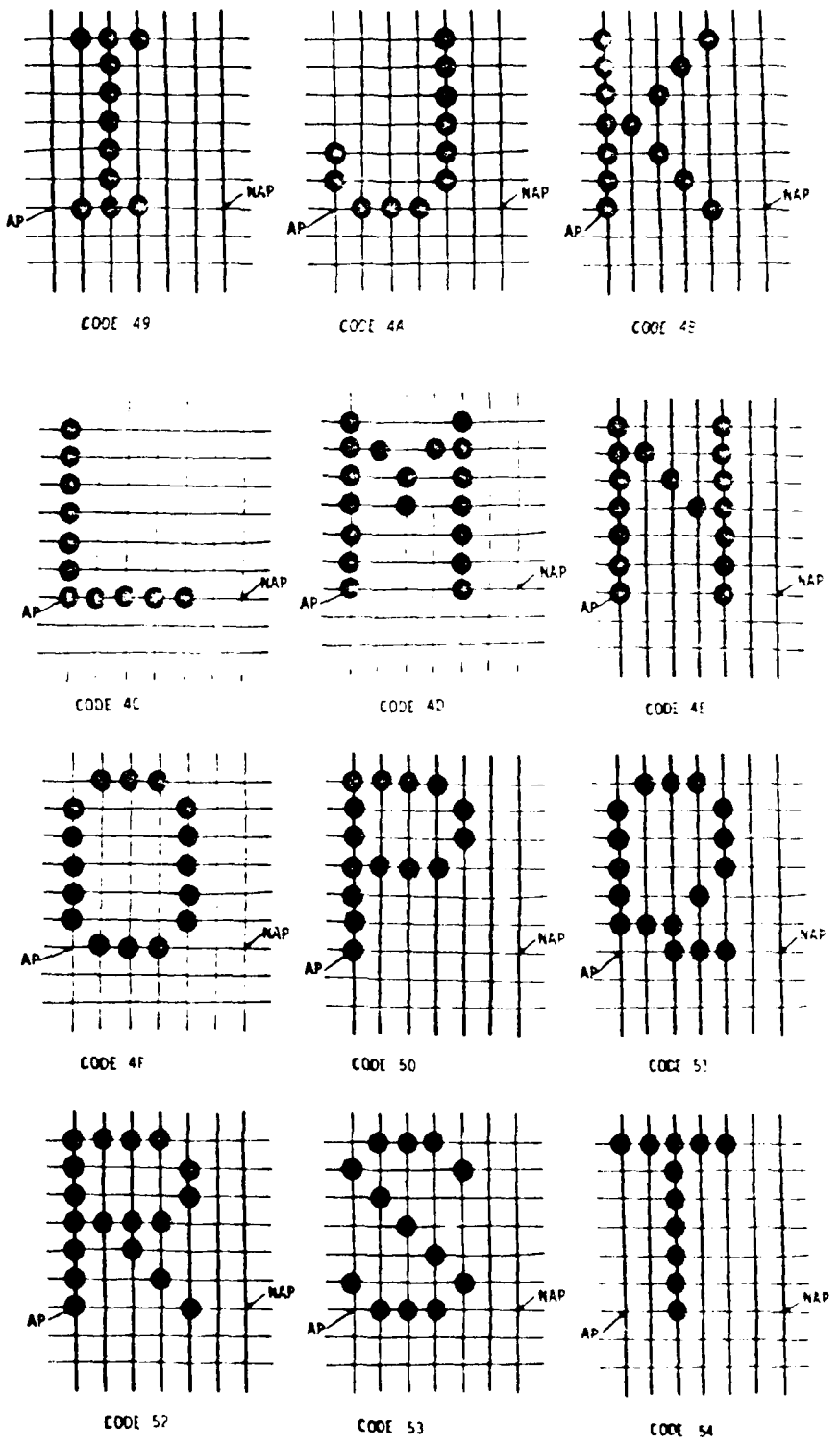


Figure 3.1.8-2: CHARACTER AND SYMBOL FORMATS (CONTINUED)

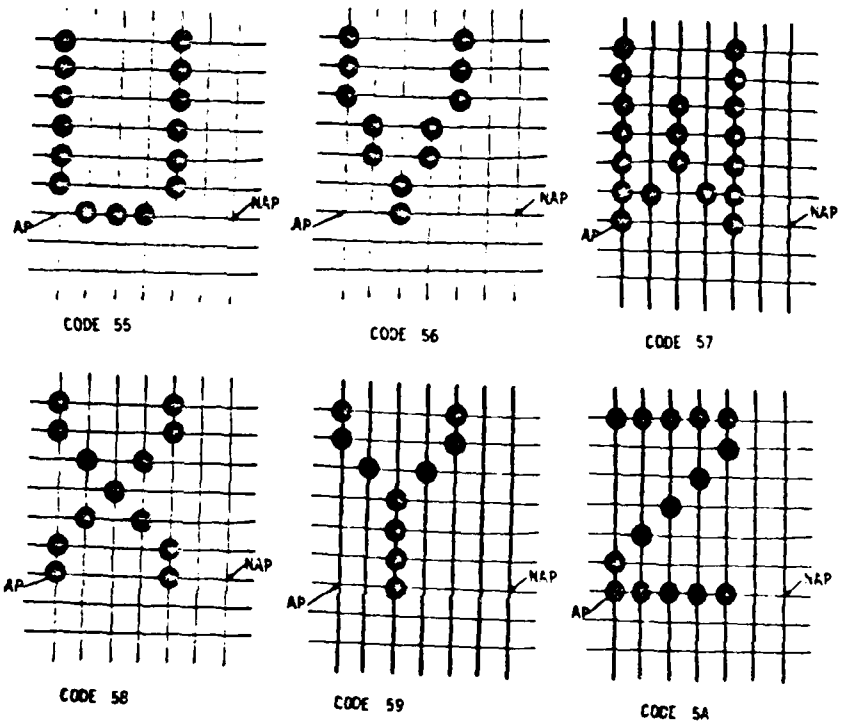


Figure 3.1.8-2: **CHARACTER AND SYMBOL FORMATS (CONTINUED)**

3.2 Mechanical Evaluations

Mechanical evaluations of the PPS units were carried out to verify the operation of the switches with respect to the activation surface and tactile feel. Additional mechanical considerations are discussed in sections 3.3 and 3.4.

3.2.1 Activation Surface

Two designs were considered for the activation surface of the PPS modules. The overall mechanical layout of the PPS module is shown in Figure 3.2.1-1. In Figure 3.2.1-2(a), one of the designs for the switch activation area is shown as a cross-hatched area. The advantages of this limited activation area are: 1) the ability to fix the filter area which covers the display and hence reduce the area requiring mobile sealing and 2) permitting the operator to view the legend when activating the switch.

In Figure 3.2.1-2(b) the alternate design for activation area is shown in the cross hatched area. In this design the operator can activate the switch by pressing on the display surface or the lower bezel area. The activation surface is pivoted near the top of the bezel and thus the activation force required is greater pressing on the display relative to pressing on the lower part of the bezel. Although the sealing requirements are more difficult, the second design was judged to be a better choice because of the larger activation surface and because of the visual cue for activation presented by the capability of pressing the lighted display area directly.

3.2.2 Tactile Feel

Tactile feel was incorporated in the switch by the use of a "buckling beam" mechanism. The mechanism includes a positive stop after the drop in resistance of the force curve. The activation force curve is shown in Figure 3.2.2-1. The cross-hatched area represents the range of force which can be expected in the PPS units as currently configured. Using this design, the force constants of the switch can be modified during manufacture to provide a higher or lower range of forces for differing applications or operator clothing.

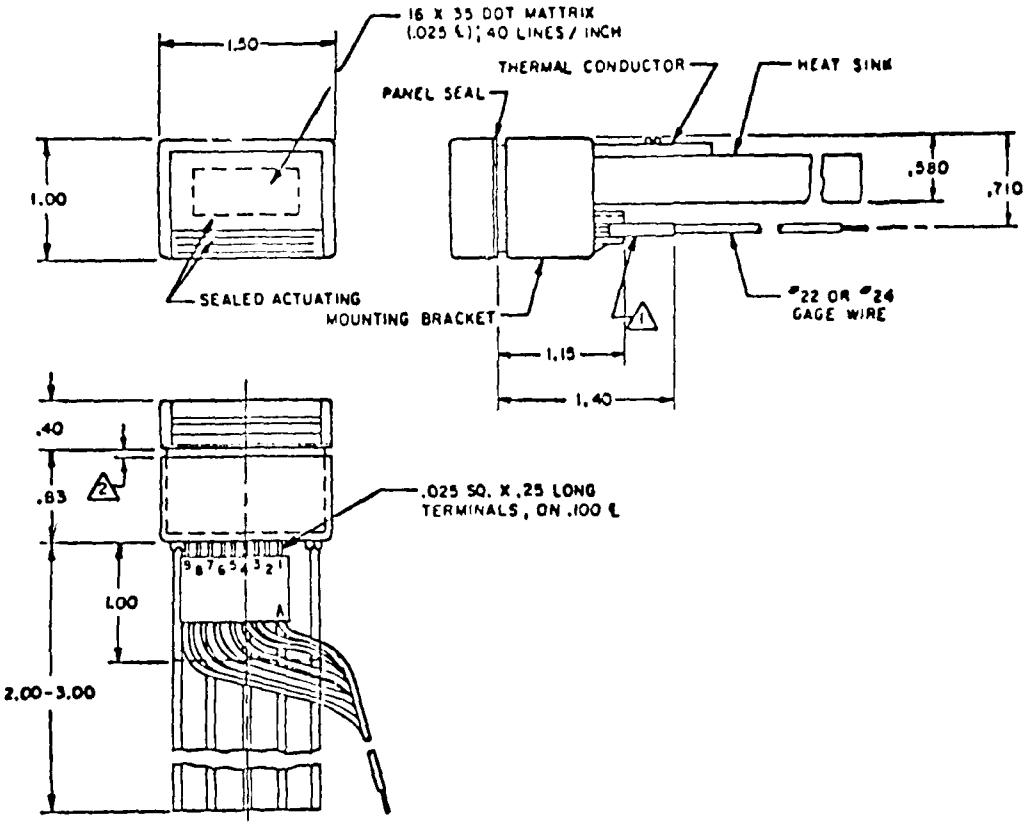


Figure 3.2.1-1: PPS Mechanical Schematic Diagram

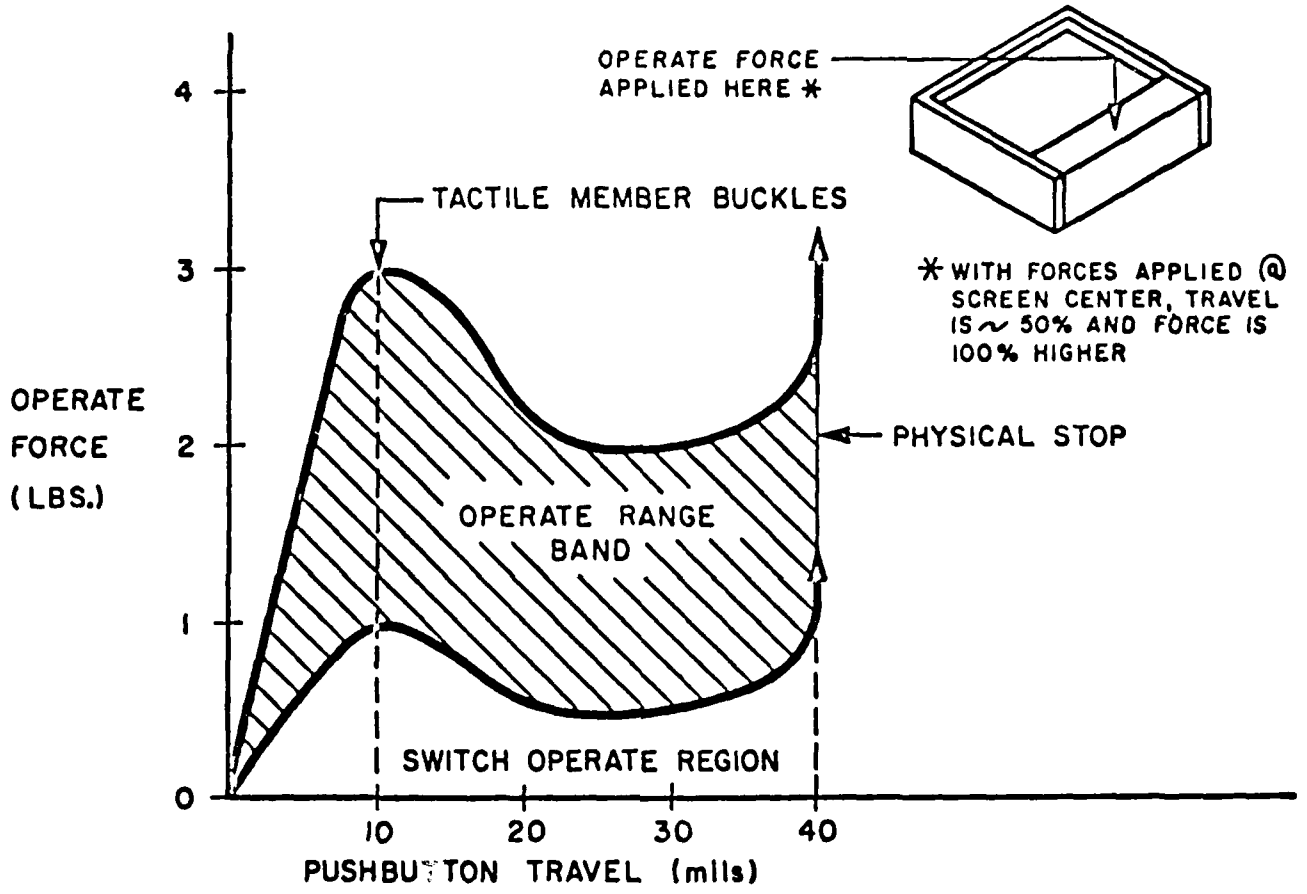
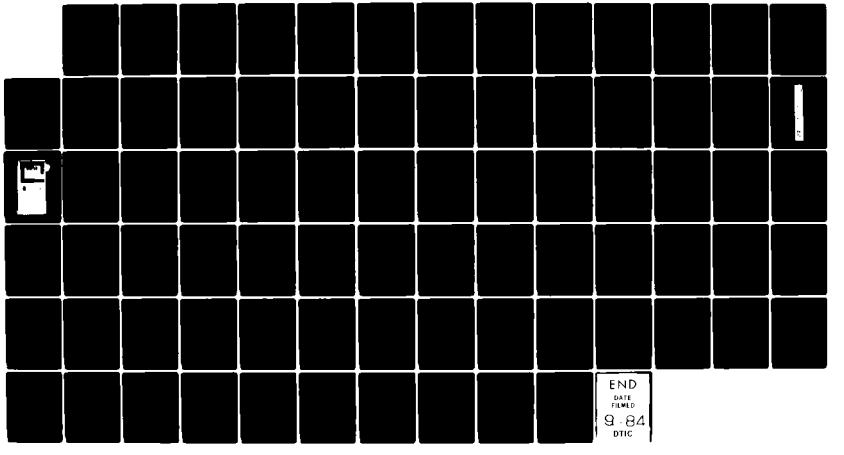
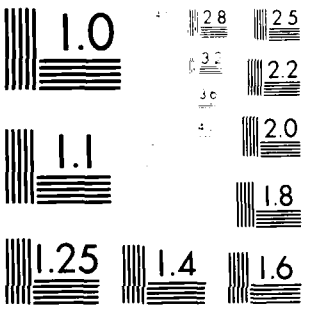


Figure 3.2.2-1: SWITCH TACTILE FEEL FORCE CURVE (EXPECTED RANGE)

AD-A145 199 LED MULTIFUNCTION KEYBOARD ENGINEERING STUDY(U) BOEING AEROSPACE CO SEATTLE WA R J SPIGER ET AL. JAN 84 AFWAL-TR-83-3065 2/2

UNCLASSIFIED F/G 9/2 NL





(a) (b)

Figure 3.2.1-2: PPS Activation Surface

3.3 Environmental Tests

Environmental testing was carried out using a sample of 5 PPS switches. Included in the tests were temperature, vibration, shock, altitude and humidity tests. The following subsections describe the test procedures and results.

3.3.1 Temperature and Altitude

The five PPS units were tested under variation of both pressure and altitude in a sealed enclosure within a circulating air chamber capable of maintaining ambient temperatures within the range determined by the test specification. The samples were tested in accordance with MIL-STD-810B, Method 504, Procedure I and the Micro Switch Evaluation Laboratory procedure. The sealed enclosure was connected to a vacuum pump and manometer to vary and measure the effective altitude. A five channel Doric digital thermometer was used to monitor thermocouple temperatures at three points on each switch (the lens, the LED substrate and the thermal conductor, see Figure 2.6.3-1b). Heatsinks were used on all samples. Testing was carried out in accordance with the steps shown in Table 3.3.1-1a.

In samples 3, 4 and 5 the supply voltage was varied during testing to determine the minimum operating voltage at each temperature and the temperature range through which the switch would function using the minimum rated supply voltage. The displays were visually monitored during the testing to insure that the LED array remained lighted and constant in brightness. Any flickering or intermittent operation of the display was reason for failure of the test.

Sample 1 operated correctly at 5VDC supply voltage over the entire temperature range. Measurements at high altitude show a slight temperature rise (less than 2°C) over site pressure. The same test was used for Sample 2. For this sample, high altitude caused little or no temperature rise (less than 0.3°C) at 25°C ambient and a rise in temperature (less than 3.6°C) at low temperature (0°C). At high temperature the switch temperatures were lower (1.1 - 1.2°C) at high altitude.

Sample 3 test results are shown in Table 3.3.1-1b. The supply voltage was raised beyond 5.0VDC at low temperature to keep the switch operational. This sample shows a temperature increase at high altitude for all temperatures.

TABLE 3.3.1-1a

TEMPERATURE ALTITUDE VARIATION

STEP	TEMPERATURE °C	ALTITUDE (FT)	DURATION (HOURS)	VOLTAGE (VDC)
1	25	SITE	0	0
2	25	SITE	1	5
3	25	40,000	1	5
4	-40	SITE	2	5
5	-40	40,000	2	5
6	0	STIE	*	5
7	0	10,000	1	5
8	25	SITE	1	5
9	55	SITE	20	5
10	55	10,000	4	5
11	25	SITE	4	5

Table 3.3.1-1b

TEMPERATURE ALTITUDE TEST OF PPS SAMPLE 3

TEMP. (°C)	ALTITUDE (FT.)	SUBSTRATE TEMP. (°C)	LENS TEMP. (°C)	THERMAL CONDUCTOR (°C)	MINIMUM OPERATING VOLTAGE (VDC)	POWER APPLIED (VDC)
25	SITE	34.2	31.5	29.7		5.0
25	40,000	35.4	32.7	30.8		5.0
-25	SITE	-23.7	-24.0	-24.3	5.3	5.3
-40	SITE	-28.7	-33.0	-35.7	5.7	5.7
-40	40,000	-28.1	-32.5	-35.5		5.0
0	SITE	18.4	13.8	9.9	4.9	5.0
0	10,000	11.3	8.6	6.4		5.0
25	SITE	38.5	35.5	32.9		5.0
55	SITE	62.5	60.2	58.4	4.5	5.0
55	10,000	62.9	60.4	58.4		5.0
25	SITE	29.7	27.0	27.1		5.0

Sample 4 also required an increase in supply voltage (5.1VDC) at -40°C. At low and room temperatures, the switch showed a temperature decrease with altitude. At high temperature, little or no increase was noted. The substrate temperature was not monitored during this test due to thermocouple failure. Sample 5 also required an increased supply voltage (5.6 and 6.6VDC) at -25° and -40°C. At low and room temperatures the switch temperatures increased slightly or remained stable with altitude. At high temperature the switch temperature decreased at high altitude (o.4°C).

3.3.2 Thermal Shock

The thermal shock tests were performed in accordance with MIL-STD-810B, method 503, Procedure I.

The five samples were subjected to the testing of this paragraph. This test was conducted to determine the resistance of the part to exposures at extremes of high and low temperature, and to the shock of alternate exposures to these extremes.

An automatic temperature shock machine having separate chambers was used for the extreme temperature conditions of steps 1 and 3 below. The air temperature of the two chambers was held at each of the extreme temperatures by means of circulating air fans and sufficient hot-cold thermal capacity so that the internal ambient temperature recovered to the specified temperature within 2 minutes after the specimens had been transferred to the appropriate chamber.

The samples were placed loosely in the transfer basket of the machine. The large mesh of the basket insured that the flow of air around the specimens under test was unobstructed. The transfer from one chamber to the other was done automatically by a motor driven mechanism that transferred the basket from chamber to chamber.

The test was performed by completing 3 cycles of the following 4-step procedure.

Step	Temperature (°C)	Time
1	-40	4 hrs.
2	25	5 min.
3	+65	4 hrs.
4	25	5 min.

Neither the supply voltage or load circuit was connected to the samples during this test. The final electrical measurements were taken within 2 hours from the end of the test at approximately 25°C. The supply voltage for the electrical characteristics measurements was 5.0 VDC. All samples successfully completed this testing. No significant changes in the electrical characteristics were observed as a result of this test and all measurements were observed to remain within specification. The display was visually monitored before and after the testing to insure that the LED array remained lighted and of constant brightness. Any flickering or intermittent operation of the display would have been considered a failure.

3.3.3 Vibration

The five switches were vibration tested in accordance with Method 204D of MIL-STD-202F, Test Condition C. Part 1 of this procedure is the same as Method 201 of the same standard.

Test Procedure:

Switches were subjected to the testing of this paragraph in the sequence shown in Table 3.3.3-1. The tests specified are intended to determine the effect on component parts of vibration in the frequency ranges that may be encountered during field service.

The test switch was mounted by its normal means to a fixture which provides a rigid mounting and is designed to have no natural resonance in the test frequency range. The fixture was then mounted directly to the vibration exciter.

Part 1

The switch was subjected to a simple harmonic motion having an amplitude of 0.03 inch (0.06 inch double amplitude maximum total excursion). The frequency was varied uniformly between the approximate limits of 10 and 55 Hz. The entire frequency range, from 10 to 55 Hz. and return to 10 Hz. was traversed in approximately 1 minute. These vibration conditions were maintained for a period of 2 hours in each of the 3 major axes for a total vibration time of 6 hours.

Part 2

The switch was subjected to a simple harmonic motion having an amplitude varied to maintain a constant peak acceleration of 10g. The frequency was varied logarithmically between the approximate limits of 55 and 2,000 Hz. The entire frequency range of 55 to 2,000 Hz (no return sweep) was traversed in 35 $\pm$ 5 minutes. The above rate may be decreased if the sample appears to be in the vicinity of resonance and if it would be helpful to facilitate the establishment of a resonant frequency. If resonance was detected, the sample was vibrated for 5 minutes at each critical resonant frequency observed. A critical resonant frequency is that frequency at which any point on the specimen is observed to have a maximum amplitude more than twice that of the support points. One sweep was performed in each of the three mutually perpendicular directions according to this procedure.

The output circuitry of the test switch was monitored throughout the test using an electronic chatter detector through a transistor interface. This equipment will detect any momentary change of state of the switch output of 1 microsecond or greater in duration. The switch was connected in the normal manner during this test except the transistor interface was connected to the output lead and served as the switch load. The switch was held deactuated during the test.

Two samples were tested with heatsinks attached and 3 samples were tested without heatsinks. The display was visually monitored during the testing to insure that the LED array remained lighted and of constant brightness. Any flickering or intermittent operation of the display was reason for failure of the test.

Switch operating characteristics were measured initially and following the vibration test. Following the test the sample was examined for evidence of broken, deformed, displaced or loose parts. Any evidence of such damage, failure to operate, substantial change of operating characteristics, or change of state of the switch output during the vibration was reason for failure of the test.

The switches completed both parts of the vibration test satisfactorily. No change of state of the switch output over one microsecond was detected on any test sample during the test. No mechanical damage to the switches was detected and the switches were operable at the completion of the test.

Table 3.3.3-1 lists the samples by number and what conditions each sample was subjected to during the test.

Table 3.3.3-1

Vibration Test Conditions

Sample	Heat Sink	Part I	Part II	Results
1	yes	yes	yes	pass
2	no	yes	no	pass
3	no	yes	yes	pass
4	no	yes	no	pass
5	yes	yes	no	pass

3.3.4 Shock

The shock test was peformed in accordance with MIL-STD-810B, Method 516, Procedure I.

The five test switches were rigidly mounted by their normal means, to an aluminum angle bracket, which in turn, was rigidly mounted on the carriage of the shock tester. The switches were held deactuated and were connected through a transistor interface to an electronic chatter detector capable of detecting an output change of 10 microseconds or more. The switches were subjected to three shock pulses having a half-sine wave form of 15 g's peak (sample 3 had 30 g's peak) and a duration of 11 milliseconds in each direction of the 3 major axes for a total of 18 drops. The output

of an accelerometer, mounted on the carriage, was fed through an amplifier to an oscilloscope.

The wave form of each shock pluse was observed to insure that it was of the required dimensions. Output change in excess of 10 microseconds was considered failure. At the completion of the test the switches were examined for breakage, loosening or visual damage. Any degradation of the samples caused by this test would be considered failure of the test.

The display was visually monitored during the testing to insure that the LED array remained lighted and of constant brightness. Any flickering or intermittent operation of the display was cause for failure of the test.

Two samples were tested with the heat sink attached and three samples were tested without heatsinks.

The samples passed this test. No change of state of the switch output of 10 microseconds or greater was detected and no visible damage or deterioration was observed upon completion of the test. Table 3.3.4-1 lists the conditions under which each sample was tested and the results of the tests.

TABLE 3.3.4-1
SHOCK TEST CONDITIONS

Sample	Shock Force (G's)	Heat Sink	Results	Display
1	15	Yes	Pass	OK
2	15	No	Pass	OK
3	30	No	Pass	OK
4	15	No	Pass	OK
5	15	Yes	Pass	OK

3.3.5 Humidity

The humidity test was performed in accordance with MIL-STD-810B, Method 507, Procedure I on four PPS samples. Before the humitity test was started the insulation resistance and operating characteristics were measured.

The switches were placed in the chamber and the temperature and relative humidity were raised to 65° and 95 percent RH over a period of 2 hours. These conditions were held for 6 hours. The chamber temperature was then reduced at a constant rate to 30°C in 16 hours while holding the relative humidity at 85% or greater. The above 24 hour sequence was run for 10 consecutive cycles for a total of 240 hours (10 days). At the end of the last cycle the samples were removed from the chamber and within one hour were measured, operated, and examined for deterioration.

Any failure to operate normally following the test or any operating characteristics or electrical measurements not within the specified limits was reason for failure of the test. Any corrosion or deterioration that would impair normal operation was considered cause for failure. The switch mounting means were also examined. Any corrosion, rust, or other deterioration that would cause jamming or freezing of mounting nuts, screws, or other hardware was reason for failure of the test.

Three switches successfully completed the humidity test. No corrosion or deterioration was noted and the switches completed the test without having the operating characteristics exceed the specified limits. There was no insulation resistance measurement less than the specified minimum value recorded following the humidity test.

Sample 2 did not complete the humidity test without incurring some damage. The Hall effect output no longer functioned upon completion of the test. Failure analysis conducted on the test sample showed that the mechanical components of the switch functioned properly and that the problem encountered was solely within the Hall chip itself and probably not caused by the humidity test.

Refer to Table 3.3.5-1 for the initial and final operating characteristics.

Table 3.3.5-1
INSULATION RESISTANCE

Sample	Insulation Resistance Initial	Insulation Resistance Final
2	500K	50K
3	500K	50K
4	500K	16K
5	500K	36K

3.3.6 Seal Test

The four samples were subjected to a seal test according to the owing Evaluation Laboratory Procedure. The purpose of this test is to determine if ·· dental spills of liquids on the surface of the display lens will penetrate into the circuit area.

The switches were mounted by their normal mounting means through mounting holes in the lid of a water tight enclosure. The switch face was on the outside. The switch and container were placed in a circulating air chamber with an ambient temperature of 55°C for 30 minutes. The enclosure was removed from the oven and oriented so that the plane of the PPS display lens was in a horizontal position. Six ounces of tap water was poured directly onto the lens while actuating the switch 3 times. The switch was actuated 3 more times after the pouring was completed.

The samples were visually inspected for signs of leakage or evidence of water inside the sealed enclosure, dielectric withstanding voltage and insulation resistance tests were performed after the visual inspection. Any visual signs of leakage or failure to successfully complete the dielectric withstanding voltage or insulation resistance tests was cause for failure of the test.

All four samples failed to complete the seal test successfully. Samples 1 and 3 leaked a total of 3 cc's of water during the test. Samples 4 and 5 leaked a total of 5 cc's of water during the test. The samples were tested in pairs so the water per individual

sample cannot be accurately determined. Sample 4 was measured for insulation resistance and dielectric withstanding voltage upon completion of the test. Insulation resistance was less that 1 megohm and the dielectric withstanding voltage was less than 50 VRMS when 500 microamps of current flowed through the sample. The samples were dried out for 16 hours at 55°C. The final measurements were then taken and found to be within specification.

3.3.7 Mechanical Life

Four samples were subjected to a mechanical life test in accordance with the following Micro Switch Evaluation Laboratory procedure. This test was performed to determine the maximum number of mechanical operations to which the samples could be subjected before any significant damage or characteristics degradation would occur. This testing was performed under normal room ambient conditions at approximately 25°C. The test specified was a one million operation, room temperature, mechanical endurance test. The samples were mounted by the normal mounting means to an aluminum angle bracket which was in turn mounted on a linear actuating machine. The angle bracket thickness was 0.190 inches and the rectangular mounting hole in the bracket was 1.400 inches by 0.900 inches in dimension.

The applied actuation was linear from release to full overtravel at a rate of 60 operations per minute. The spring loaded actuators used were adjusted to give an end force of 2 pounds. The actuators must be depressed by 0.240 inches to produce the 2 pound end force. The plunger of the actuator was a soft rubber actuator having a hemispherical shape with a radius of 0.250 inches. The actuators were adjusted on the actuator arm to cause the center of the rubber actuator to contact the test device push bar directly at the center. There were no electrical connections made to the samples during this test.

The operating force measurement and travel characteristics of the test samples were checked at periodic measurement intervals to determine the effect of continuous actuation of the device mechanism. There was no criteria for failure established for this test. The test was an investigation to determine the wear-out characteristics of the test samples.

Two samples were subjected to a total of one million mechanical operations. The remaining samples were subjected to 500,000 mechanical operations. The wear experienced on the filter actuation tip was a significant problem area during this test. This wear caused the required operating force to increase approximately two-fold after the accumulation of 250,000 consecutive operations. The lens was therefore changed at several measurement intervals to continue this test.

4.0 MFK SYSTEM INTEGRATION

The third major phase of this study was the incorporation of the PPS/LRCU units into a simulation of an MFK system to test their operation under realistic conditions of switch activation and data and command transfer. The MFK controller chosen was actually a full-fledged controller developed in a parallel Boeing effort. The evaluations and tests conducted are therefore considered valid for a complete keyboard configuration of as many as 28 PPS units.

4.1 System Design Features

A number of useful features of a MFK system are described in section 2. These features have been incorporated into the MFK controller and the associated data base where possible. These features and some other aspects of the MFK test system are described in the following subsections.

4.1.1 Operator Procedure Storage and Cueing

The MFK operating system was programmed to initiate a cued operator procedure by means of a series of blinking switches. Upon receiving a message from the host computer, the MFK controller cycled through a stored procedure. The operator was cued to each step in the procedure by a blinking switch on the appropriate switch of the four switch array. This routine is shown in detail in the four switch data base in Appendix A. This routine demonstrated the initiation of an operator procedure by a cueing message from the host. Such a message could result from a caution and warning situation or from a predetermined set of parameters (e.g., reaching cruise altitude).

4.1.2 Scratchpad Data Display

In surveying applications of a MFK system, a common thread was found to be a need for processing checklists and procedures consisting of a number of steps. The use of a scratchpad display capable of 10-20 lines of information was found to be extremely useful for this purpose. As a result, this type of scratchpad capability was incorporated into the plans for the MFK controller. For initial work a Sharp thin film

electroluminescent (TFEL) panel with both alphanumeric and graphics capability was employed.

4.1.3 MFK Architecture

The MFK test system developed uses a modular concept which permits a relatively simple adaption of the system to a variety of switch configurations making up the keyboard. For example the keyboard can be made up of anywhere from one to 32 switches depending on initial conditions loaded into the operating system. (Operating speeds remain constant up to 20 switches.)

4.1.3.1 Controller-Keyboard Interface Architecture

Both parallel and serial data links between the controller and keyboard were considered. To locate the PPS/LRCU units remotely from the controller, a line capable of driving over some distance and minimizing the number of wires was required. A requirement for a minimum operating distance capability of 25 feet was decided upon based on considerations of cockpit size and cable routing. Within this constraint, candidate options were an RS-422 or RS-232 link. The RS-422 was chosen because of its single voltage power supply requirement and a 200 foot limitation of the RS-232 interface. The RS-422 link is capable of driving over 1,000 feet of line. The serial version was chosen over parallel to reduce the number of wires (6 vs. 24 per LRCU). A 19.2Kb/s data rate was found to be sufficient to achieve the required switch updata times unless more than two full graphic symbols per LRCU are used. The RS-422 serial interface was chosen because of its long line driving capabilities, low number of wires and single 5 volt power requirements. With this interface, only one voltage is needed to power the LRCU and PPS modules. The software link between the controller and keyboard must match the resident firmware on the LRCU. The commands to which the LRCU responds and the data transfer options are listed in detail in Section 2. Both alphanumeric legends and graphic symbols are supported by the interface. The baud rate between controller and keyboard is programmable.

4.1.3.2 Controller Architecture

The controller uses an Intel 8-bit 8085 based processor and communicates with memory and I/O devices over a multibus. This structure allows a variety of I/O devices to be added to the system depending on keyboard size and auxilliary display types required. This tradeoff is heavily system dependent and a large display requirement may require additional processing power. Resident in the controller is a basic operating system which handles the initialization, command processing, communication and luminance control (see Section 2.6). This software system operates independently of the data base and thus allows a variety of data bases to be used in the MFK. The data bases contain the stored legends, display commands and logic trees associated with the page structure. Storage of the operating system requires 8Kb of EPROM with additional 4Kb of RAM being required for system operation. The data base storage requirements are application dependent. A full display of alphanumeric data on the TFEL display (480 characters) requires 0.5Kbytes of storage. A full graphic display would require 10Kbits. Storage requirements per switch legend vary from 6 to 86 bytes, depending on legend complexity. A typical data page (see Section 2.6) for twenty switches would require 69 types of storage.

4.1.3.3 Host-Controller Interface Architecture

The host-controller link was defined in the study as an RS-232 link to enable interfacing easily to a variety of host computers. The command structure between controller and host is similar to that between the controller and LRCU with sumchecks being used to verify data integrity. The host controller link can be set to operate at a variety of preselected baud rates up to 9.6Kb/s.

4.1.4 Luminance Control

The LRCU as currently configured responds to commands for 37 levels of luminance control. To operate these levels a luminance sensor was constructed and interfaced to the controller. The sensor output was sampled periodically 12 Hz and converted to a digital integer. This portion of the luminance control operated automatically. A manual potentiometer provided a luminance adjustment option and its input also was converted to a digital integer. These two values were then combined to access a look-

up table which determined the appropriate luminance step command to send to the LRCU. The look-up table, although somewhat cumbersome, permitted a high degree of flexibility with respect to the relative magnitudes of the automatic and manual portions of the control. The automatic sensor was set to approximate the midrange of the control region as shown in Figure 3.1.1-5. The basic objective of the luminance control testing was to establish the ability to control the luminance levels in the PPS/LRCU design and to determine the validity of step size choice and range of steps.

4.2 Keyboard Controller and Scratchpad-Controller Interface Evaluations

Evaluation of the keyboard-controller and scratchpad-controller interfaces involved calculations of estimated operating times coupled with actual operating time measurements.

4.2.1 Calculated Operating Times

Operating times for the command and data transfers necessary to update the keyboard and scratchpad displays were calculated using a representative mix of software instructions for several combinations of processors and hardware interfaces. A serial RS-422 line operating at 19.2 Kb/s was chosen as the interface from the controller to the keyboard. Figure 4.2.1-1 shows the calculated operating speed for both alphanumerics and bit map graphics patterns for two choices of controller processor. Representative examples chosen were the Intel 8085 (8 bit) and 8086 (16 bit). Initial estimates indicated that the 8085 would be sufficient for switch numbers 20. Above this number, the system is no longer transmission limited and the faster processing of the 8086 results in increased speed. Since many applications are planned for 12 to 20 switches, the 8085 option was chosen based on previous experience with this microprocessor. To perform the calculations, sample interface software was defined and the time necessary to perform the instructions was calculated. The vertical portion of the curves in Figure 4.2.1-1 represent the transmission limitation of the 19.2Kb/s line. The diagnoal portion shows the effect of additional switches on processing time to provide data to the output registers.

A similar calculation was carried out for the interface to the TFEL scratchpad display. These results are shown in Figure 4.2.1-2. Use of an I/O serial port was deemed to be

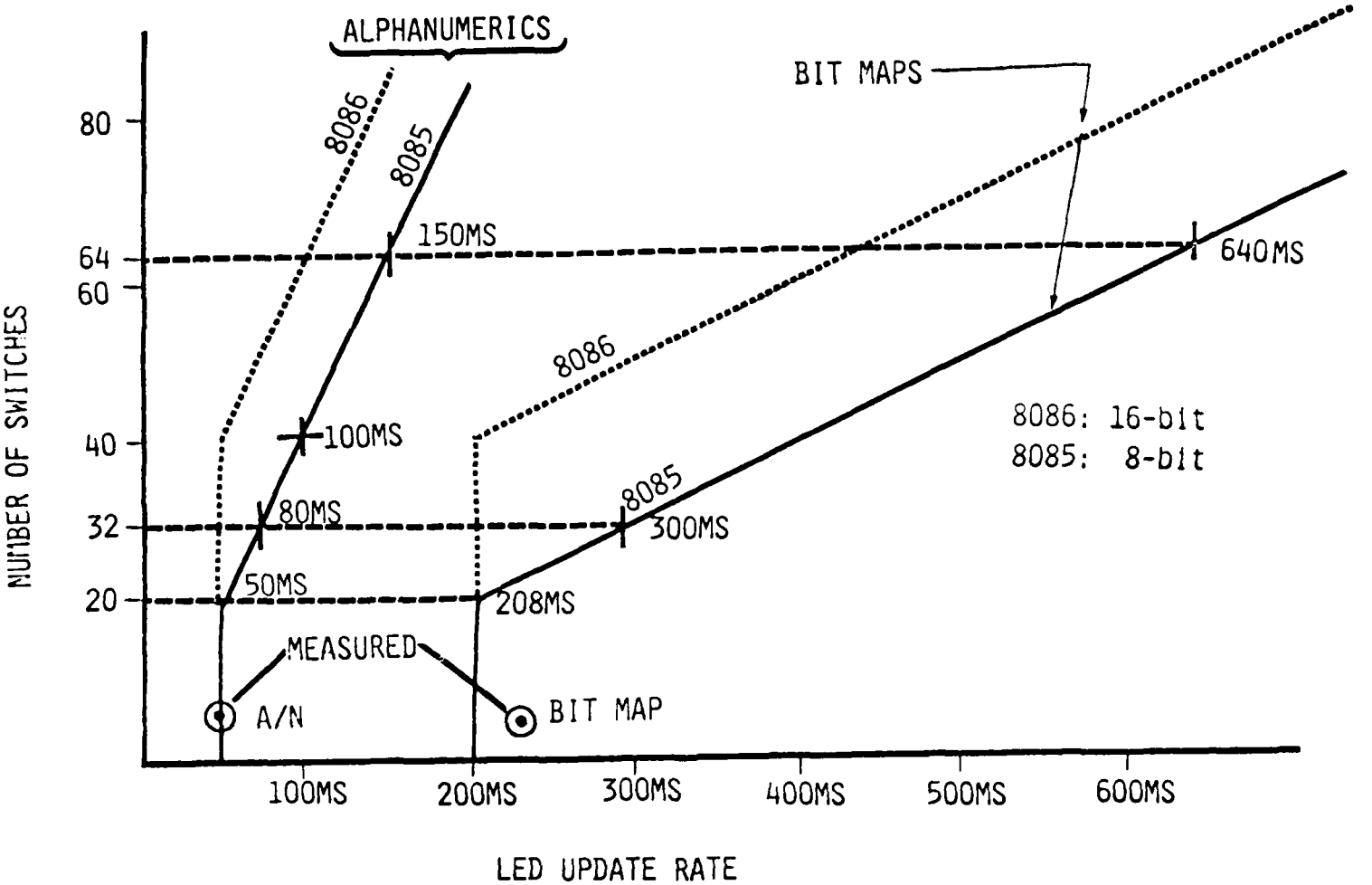


Figure 4.2.1-1: LED MFK UPDATE VS NUMBER OF SWITCHES

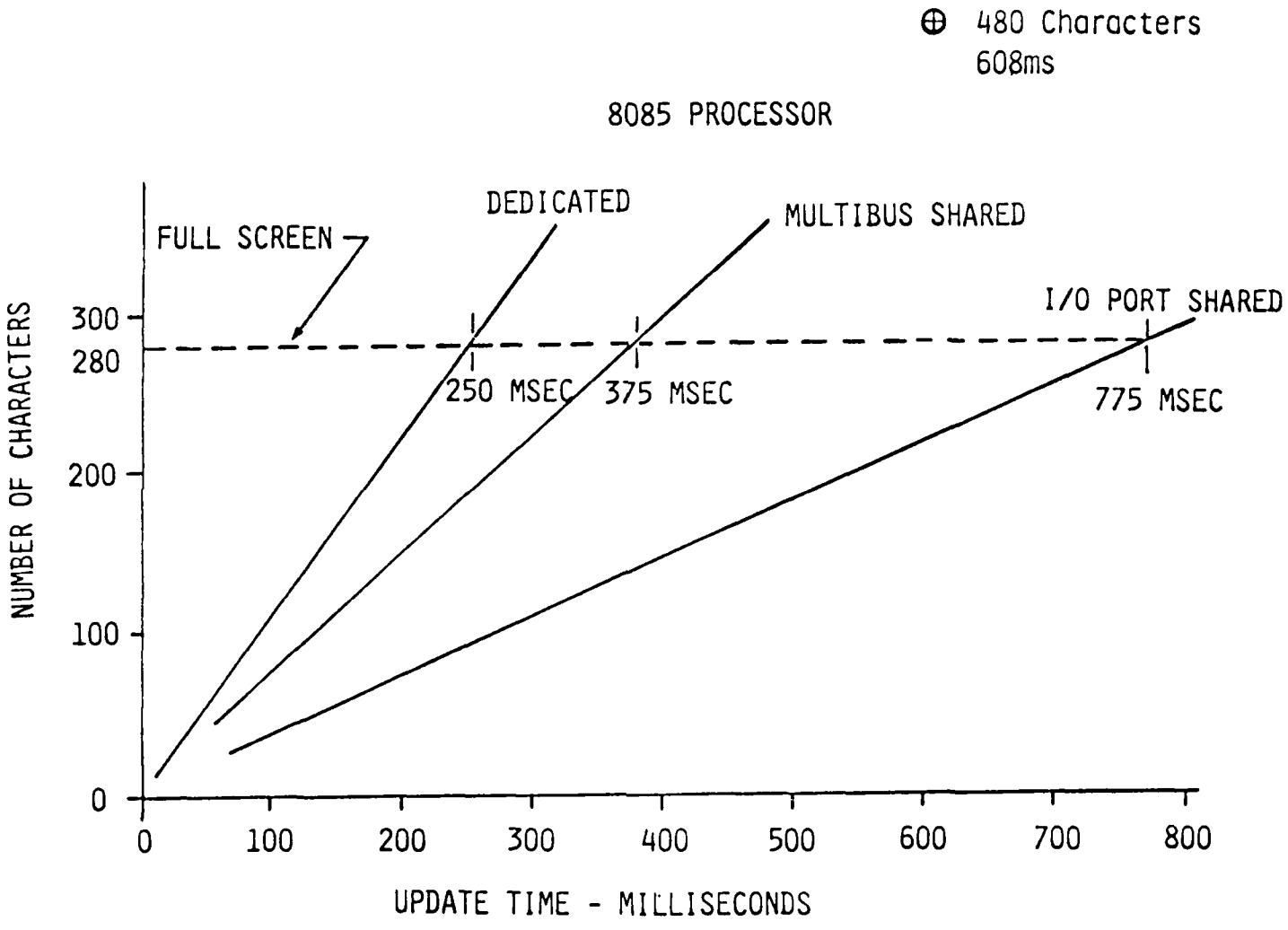


Figure 4.2.1-2: TFEL ALPHANUMERIC DIAPLAY UPDATE RATE

too slow relative to the other options shown in the figure. A shared multibus configuration was chosen to eliminate the need for another processor.

In both latter cases, the estimate of update times was within the goals established as part of the system requirements (200 msec for the keyboard and 800 msec for the scratchpad display).

4.2.2 Measurements of Operating Times

Actual operating times were measured for the 8085 based MFK controller connected to the 4 PPS/LRCU unit and to the Sharp TFEL scratchpad display. These times are indicated as circles on Figures 4.1.2-1 and 4.2.1-2. The measurements indicate that the update time for the switch matrix will be 52 ms for a set of four switches with alphanumeric legends. A timing analysis of current software used in a 20 switch array shows that the departure from transmission limitation occurs between 16 and 20 switches for 2 rows of 6 alphanumeric characters. For bit mapped data, the measured time was 250 ms. The update goal time of <0.2 sec will then be met if two or more of the legends on switches associated with a given LRCU are displaying alpha-numeric legends.

The measurements of update time for the TFEL scratchpad display indicate an update time of 608 ms for 15 lines of 32 characters. This time is also within the goal of $<$ 800 ms for the scratchpad update time. All calculations and measurements shown were for the TFEL display. The CRT display update rate would be defined by the 9600Kb/s rate of the RS-232 cable used with the terminal in which the CRT was located. The curves shown in Figure 4.2.1-2 indicate update times for three configurations. In the first, a dedicated processor would handle the updating of the dipslays. This would add another processor to the MFK system. In the multibus shared mode (used in the controller) part of the controller RAM is mapped into the space used by the TFEL display graphics card. The shared I/O port mode would output data to the TFEL display through one of the controller I/O ports. All calculations were based on a timing analysis of the software instructions necessary to implmenet each of the three modes.

4.3 Luminance Control Evaluation

The luminance control evaluation involved the evaluation of design options for the luminance control as well as the evaluation of the luminance control function of the LRCU.

4.3.1 Luminance Control Design

The original luminance sensor design was based on a new chip design by TRW which combines a photodiode and output electronics in a single package. Tests of the chip function showed a limited dynamic range of roughly 2 orders of magnitude vs the 3.5 required for adequate control. This problem was traced in part to a design defect in the chip caused by excess gain in the current amplifier following the photodiode. The correct gain will be incorporated in the next run of the TRW chip. In addition, the response curve of the sensor was more sensitive to near-IR rather than visible light. A wider range design is currently being tested.

A basic problem forseen in the PPS/LRCU luminance step levels was the linearity of the steps. At low ambient illumination the steps are too large. The current design makes a change in step size quite difficult. As a result, no changes will be incorporated in the step number or step size until the next iteration of the PPS design. A calculation of the appropriate step size using the criteria of Reference 2-1 indicates a need for step sizes as low as 0.0004fL at very low light levels if the step transitions are to be indistinguishable by an observer.

4.3.2 Luminance Control Measurements

The luminance control system was tested on the set of four switches. For each step, the luminance of the display was measured with a photometer relative to the other steps. The results are shown in Figure 4.3.2-1. Note that the measured luminance of the top 5 steps is essentially the same. This effect is currently under investigation by microswitch. At low ambient light levels the luminance steps are too large, resulting in a noticeable jump in light output from step to step. The lowest luminance level also produces electrical crosstalk between adjacent rows of LED's on the display. This problem has been traced to the timing in the LED drive circuitry. The problem will be corrected in the next switch design iteration.

Both the automatic sensor and the manual control performed satisfactorily with the exception of the sensor dynamic range, although a wider dynamic range is needed for the luminance sensor and an increase in, and redefinition of, luminance step size. In this usage "satisifactory performance" implies that the system performed correctly within the design limitations.

4.4 System Operation Testing

A four switch data base was developed and coded directly into the MFK controller for use in testing operation of the PPL/LRCU units as part of an MFK system. The data base included displays on both the PPS units and on a CRT terminal used as a scratchpad display. The CRT display was used during this phase of testing due to unavailability of the TFEL display. Other scratchpad analysis and testing used the TFEL display. The legends and logical structure of the data base are given in Appendix A. The data base was tested in conjunction with the operating system developed for the MFK controller. The following sections describe the tests carried out as part of the study.

4.4.1 Host to MFK Data Download

An RS-232 9600 Baud serial link was established between the MFK controller and a host computer (PDP 11/70). The link was used to test the transmission of commands and data from the MFK controller to the host and the downloading of data and messages from the host to the controller. Commands and data were passed between the two computers according to a set protocol which employed a data record format (Intel Hex format). Each record contained a checksum to ensure data integrity. Figure 4.4.1-1 shows the flow of events from switch activation to the MFK reaction to the host response. Upon switch activation, data is sent from the LRCU to the controller UART which generates a controller interrupt. The controller then reads the LRCU message which provides a definition of the switch number that was activated (see Figure 4.4.1-1). The serial RS-422 link between the controller and LRCU was operated at 19.2Kb/s. If a switch activation message conflicts with an ongoing transmission between LRCU and controller, the ongoing transmission will be completed and acknowledged before the switch activation message is processed.

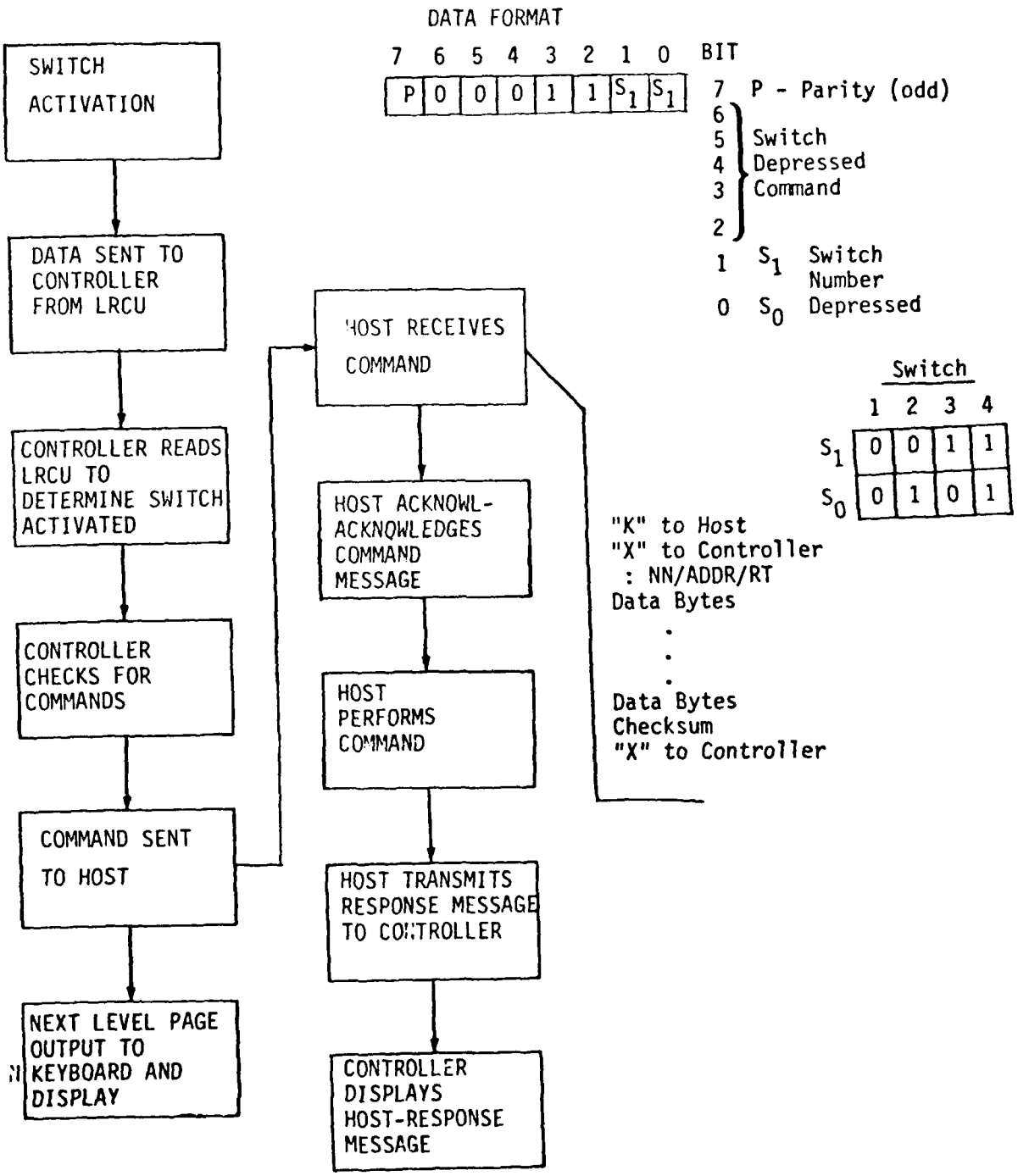


Figure 4.4.1-1: MFK SWITCH ACTIVATION FLOW DIAGRAM

Having defined the switch number depressed, the controller looks for display and host commands associated with that switch as well as the next page of legends to be displayed on the keyboard (see Figure 2.6.2.2-1).

Any command message to the host is sent via the RS-232 serial line. A data rate of 9600Kb/s was used in the test cases to conform with host I/O operations. A typical message from the controller to host processor (see Figure 2.6.2.1-1) uses the following format. A command message header work (ASCII "K") is sent to the host which responds to the I/O interrupt. The host acknowledges the command header word by sending an acknowledgement word (ASCII "X") to the controller. The controller then sends a number of data bytes in an Intel Hex record format. The number of record bytes is a user selectable variable, up to a 256 bytes maximum (see example, Figure 4.4.1-1). The record starts with an ASCII ":", followed by the two characters "NN" which define the number of data bytes. All elements of the message are formed of ASCII characters. The next four characters "ADDR" define the address to which the message is directed. The characters "RT" define the record type. "01" denotes a valid record while "01" denotes an end of record.

The DATA BYTE characters occur next and are defined in number by NN. These are followed by a checksum of all message elements after the ":" with the checksum being composed of the eight least significant bits of the binary sum of the message elements. The host verifies the data with respect to the checksum and acknowledges each record with an ASCII "X" until an end of record is received and acknowledged. The message is then processed by the host and any responses are sent to the controller using the same protocol.

Three basic tests were conducted between the MFK controller and host. First, a message was sent to the host containing display changes codes. The host was programmed to verify the message and retransmit it to the controller. Display of the appropriate information on the MFK was taken as evidence of proper command messge uploading and downloading performance over the host-controller link. The second test consisted of trhe transmission of an emergency command message from the host to controller. This command followed the format described with the exception of a change of "K" to "E" in the first ASCII character transmitted. The data bytes supplied the address of the emergency message legend page to be displayed. The third test was

designed to test the ability of the host to download information, (such as a change in data base), from the host to the controller. A test file was installed in the host and transmitted to a specific address in the controller.

The memory of the controller was then interrogated to verify that the data base had been downloaded successfully. The command and data transfer test and the data download tests were performed successfully. The host is not kept busy by the MFK except during message reception and transmission and the percentage of host time required during these periods depends on the message and response sizes. Typical values would be approximately 0.2 - 0.3% or less depending on the host capabilities for I/O handling.

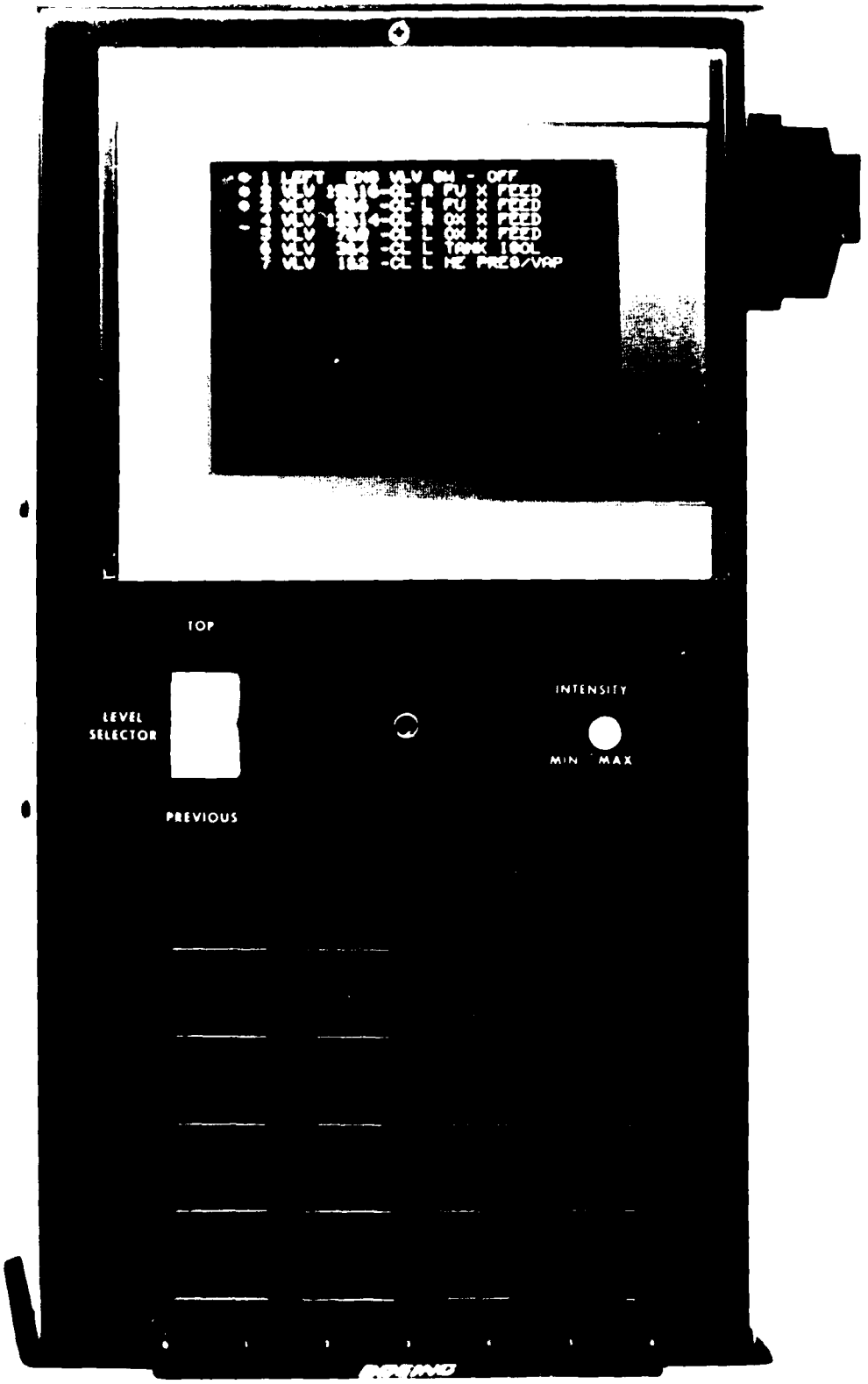
4.4.2 Legend Storage Capacity Testing and Logic Tree Response

The four switch data base shown in Appendix A was used to test the capacity of the MFK for legend storage and proper logic tree response. This data base simulated access to two systems (hydraulic and communications) and associated subsystems using several levels of indenture. All branches of the logic tree were exercised using the PPS switches and the MFK controller in conjunction with a CRT terminal used as a scratch pad. Sample legends displayed on the four switches are shown in Figure 4.4.2-1. No errors in operation, faulty logic response or faulty legend displays were detected. Although coding was done for a four switch array, the organization of the MFK controller is such that successful operation of larger switch arrays can be expected. Currently, the controller is being used successfuly to operate a 20 switch keyboard array and accompanying data base. Figure 4.4.2-2 shows the unit which also includes the Sharp TFEL panel.

4.4.3 Power Requirements and Consumption

The power consumed by the four PPS switches and the associated LRCU was measured under two conditions. The first measurement was with a 25% fraction of LED's lit on all switches or 140 out of the 560 LED total. Power consumption, voltage and current were measured for the display power to each switch and for the logic power to the LRCU and four switches. These values are shown in the top portion of Table 4.4.3-1. In the second test legends made up of 11 or 12 characters were displayed. The power,

Figure 4.4.2-1: SAMPLE LEGENDS ON FOUR SWITCH ARRAY FROM DATA BASE INVENTORY


TOP
LEVEL SELECTOR
PREVIOUS
INTENSITY
MIN
MAX

current, and voltage levels are recorded for these measurements in the lower portion of Table 4.4.3-1. Note that in general the number of LED's lit in an 11 or 12 character display exceeds 25%. For the 25% fraction of lit LED's the power/switch is ~1.3 watts. This number is below the study requirement of two watts but more than the desired goal of 1 watt. No excessive heat was noted, however, while operating the switches in an open air environment.

4.4.4 Reliability Assessment

The set of four switches performed well during the MFK system testing. One row failure occurred shortly after the switch arrival. Its intermittent behavior appears to have been a connection problem. At this time, insufficient operating time has been acquired with the PPS unit to provide reliable experimental numbers on failure rates. The major differences relative to a single function switch lie in the more complex display and the additional microprocessor linkage to the host computer. Because of the multiple functions associated with the switch, the loss of the switch display is more important than would be the case for a single function switch. However, display loss can be compensated for in other ways. Two approaches currently under consideration are 1) the option of displaying a desired page of switch functions on the scratchpad or an associated cockpit display and 2) performing a permutation of switch and display functions on the keyboard. The first would be most applicable to a case where the display fails and the switch action continues to operate. The second would also be applicable to a completely failed PPS or LRCU. The second option would, in general, compensate for the reduced reliability associated with incorporating multiple functions into a single PPS unit by providing multiple switches to perform that function.

The reliability of the microprocessor linkage to the host computer forms the other major failure factor relative to a system of single function switches. The failure of communication of switch action through the controller would render the complete keyboard inoperative. This mode of failure would require built-in redundancy in the controller to insure a sufficiently high reliability for the particular systems the MFK was controlling. This reliability level will depend on the criticality of these systems.

Switch No.	Display Pattern	Display Voltage Reading per Switch	Display Current Reading per Switch	Display Power per Switch	Total LRCU Power
1	140 LEDS	5.18 VDC	146 ma	756.3 mw	3.12W
2	140 LEDS	5.18 VDC	172 ma	891. mw	+2.0W
3	140 LEDS	5.18 VDC	146 ma	756.3 mw	=5.12W
4	140 LEDS	5.18 VDC	142 ma	735.6 mw	
1	11 alphanumeric characters	5.18 VDC	172 ma	891 mw (159 LED's)	3.76 W (Display Only)
2	11 alphanumeric characters	5.18 VDC	182 ma	942.8 mw (169 LED's)	
3	12 alphanumeric characters	5.18 VDC	196 ma	1015.3 mw (197 LED's)	
4	12 alphanumeric characters	5.18 VDC	175 ma	906.5 mw (165 LED's)	

Figure 4.4.3-1: PPS/LRCU Power Consumption Test

The ability to identify failed components should be built into the MFK. Currently, the MFK operating system and data base used in a Boeing demonstration MFK provides a test capability for the individual PPS actions and displays, the scratchpad display and, controller memory and LRCU communication with the controller.

5.0 CONCLUSIONS

Tests of the PPS/LRCU units as part of a MFK system were quite successful. Operation of the four switch set verified the operating capability of a MFK architecture based on a modular design. Transfer of data and commands between controller and host and between controller and keyboard, as described in sections 4.4.1 - 4.4.3, provided a demonstration of the capability and successful operation of the displays, the LRCU firmware, the MFK operating system and controller hardware and the command and data transmission formats. Implementation and operation of the four switch data base of Appendix A provided a verification of the correct storage of legends and proper logic tree response of the system (section 4.4.4).

In surveying applications of the MFK to either tactical or commercial aircraft, the architecture chosen was applicable to the requirements of either area. The capability of including a larger scratchpad area (10-20 lines) in the system was found to be necessary if checklists and multistep procedures are to be handled by the system. This type of display could be operated on a time-shared basis and also serve as a device for graphics display.

In considering the performance of the MFK system, the access schema associated with procedures involving multiple systems becomes cumbersome if changes between systems are frequent. The use of stored procedures and/or the automation of procedures has been identified as a means of handling these situations. The capacity for automatic or semi-automatic operation should be included as part of the MFK operating system.

Several areas of switch design and construction were identified during testing and evaluation, which require further efforts. These include luminance and luminance control, environmental protection and construction. The luminance of the discrete green LED arrays used in this evaluation were too low by a factor of approximately 2. The Flight Dynamics Laboratory (Wright Patterson AFB, Ohio) has tested LED displays from another source that are sunlight legible. The options for increasing the diode efficiency should be explored and implemented. Currently, display efforts at Micro Switch are directed towards developing production quantity suppliers of more efficient LED arrays. An estimated factor of two in LED efficiency can be achieved by mounting the 8 LED "sticks" used by OPTOTEK in an anode down configuration (present mounting is anode up). Concurrently, improved designs for the

contrast enhancement filter are being considered. The current bandpass filters produce a degree of image blurring, particularly at off normal viewing angles. This problem must be corrected while preserving the fingerprint suppression characteristics of the matte finish on the filter surface.

Testing of the PPS units in a 20 switch array has shown a very low increase in temperature under condition of 20°C ambient operation (PPS units are barely warm to the touch). The power levels of approximately 1.3 watts/switch indicate the possibility of driving the available LED's harder while staying under the design limit of 2 watts of power dissipation per switch. Luminance control steps are too large. The design should be changed to incorporate a larger number of steps and to scale the step magnitude in a logarithmic rather than a linear fashion.

The current PPS/LRCU design was not optimized with respect to operation over a wide range of temperature or humidity. Further design work should employ components to permit operation over a wider range of temperature (up to 95° C). Components should also be sealed or otherwise protected against humidity. A structure problem in the current design is the attachment of the PPS heat sink. The structure of the heat sink and the remainder of the PPS should be integrated to eliminate potential mechanical problems under vibration conditions.

Several follow-on activities to the present study are planned. The size of the switch and the pixel format of the array are limited to a large extent by the available electronics for LED drive circuitry. By developing custom circuits the display driving capability can be increased. This increase will permit the enlargement of the display matrix (e.g. a 25 x 65 array) resulting in a greater character capacity and more font options. Another option would be the use of multicolor LED displays. Ultimately, the advances in the circuitry package are expected to result in a PPS which contains in itself the function of the LRCU, thus making the PPS truly modular.

From a system aspect, a current future activity has been the construction of the 20 switch MFK system (see Figure 4.4.2-2) which includes a 320 x 240 pixel TFEL scratchpad display. This unit permits the testing of larger data bases and the simulation of a large number of potential MFK applications.

6.0 REFERENCES

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APPENDIX A

DATA BASE LOGIC STRUCTURE FOR A FOUR PPS MODULE

The following appendix contains the page and logic layout for a data base designed for a four PPS module. The data base illustrates a means of controlling two systems with the module. These are a hydraulic system and a communication/navigation system. The data base was not designed as a comprehensive demonstration of either system, but rather as a demonstration and test of the PPS/LRCU and MFK operating characteristics. The tests conducted, using the data base, are described in Section 4. Logic organization of the data base takes the basic form of a tree structure as shown in Figure A-1. The top level page is Page 1. Pages accessed by pressing one of the switches A-D on page 1 are designated by page numbers 1A, 1B, 1C and 1D. Successive page levels of the logic tree are shown by the designations listed in Figure A-1. The TOP LEVEL switch on any of the pages will return the operator to page 1.

The display area indicated in the large area at the top of each page sheet shows the alphanumeric CRT display which appears in conjunction with the keyboard display. The CRT display shows the system status as a result of switch actions and provides prompting as to the appropiate operator action.

The hydraulic system logic tree accesses three subsystems with a speed control and on/off capability for each. The communication/navigation system accesses two VHF radios and a TACAN with an on/off and frequency select feature for each. The fault function illustrates the use of a blinking switch to bring the operator's attention to an action which should be taken. In this case the hydraulic subsystem should be turned off. Selftest accesses legends indicating tests on the MFK keyboard and controller.

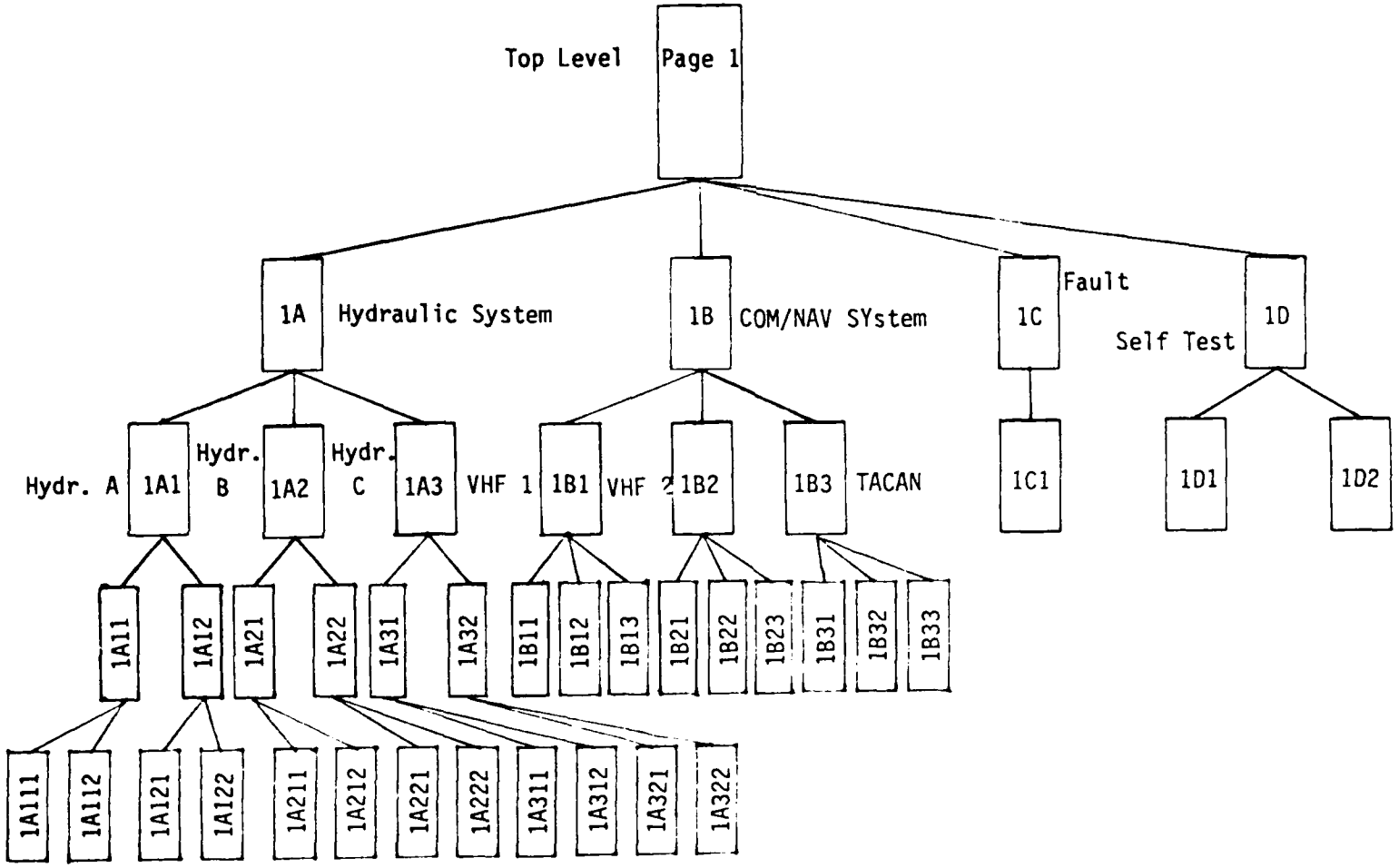
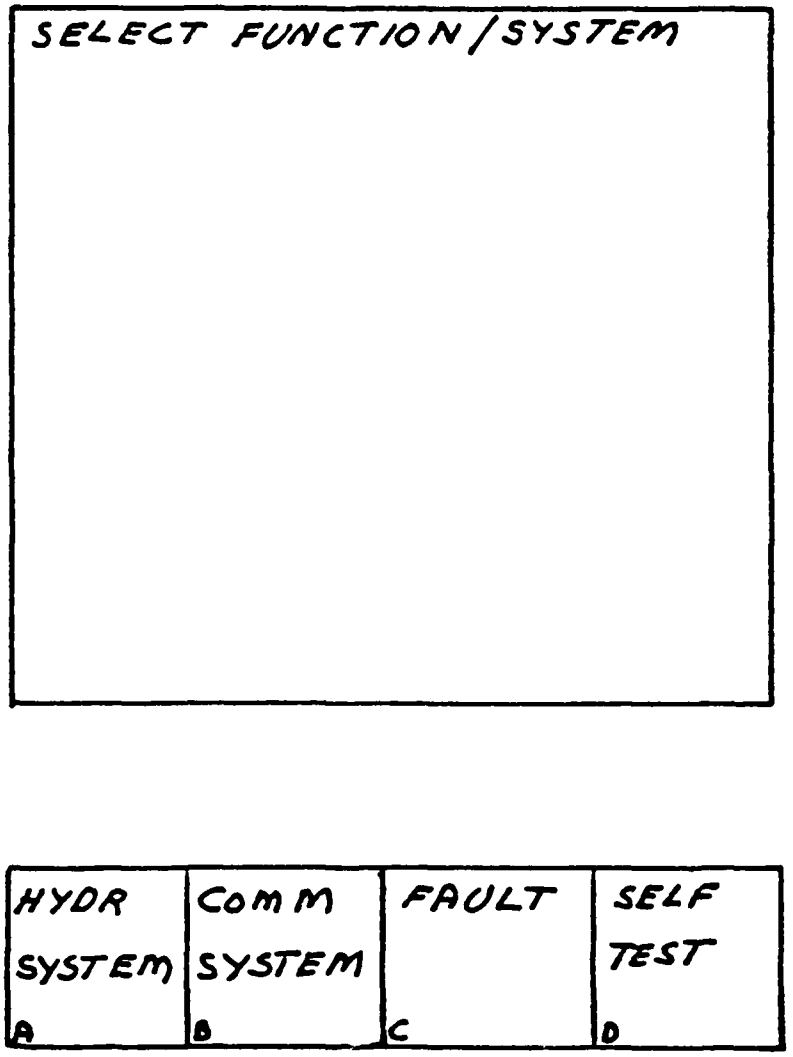
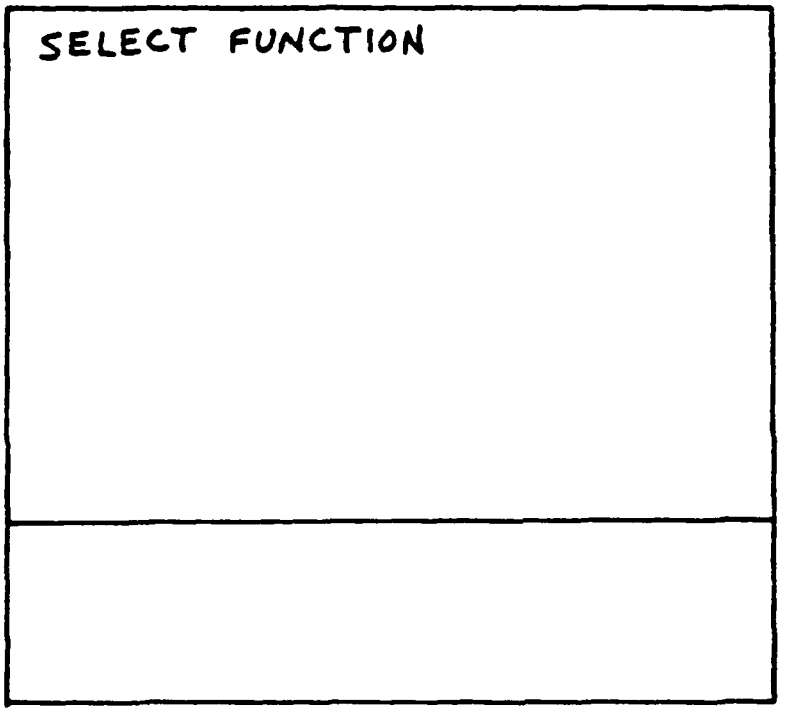
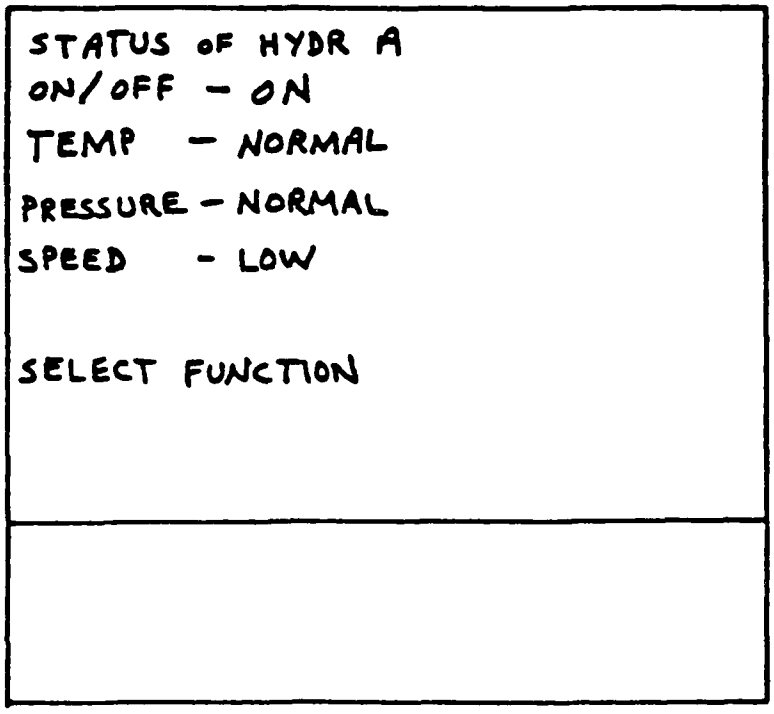


Figure A-1: FOUR SWITCH DATA BASE LOGIC TREE

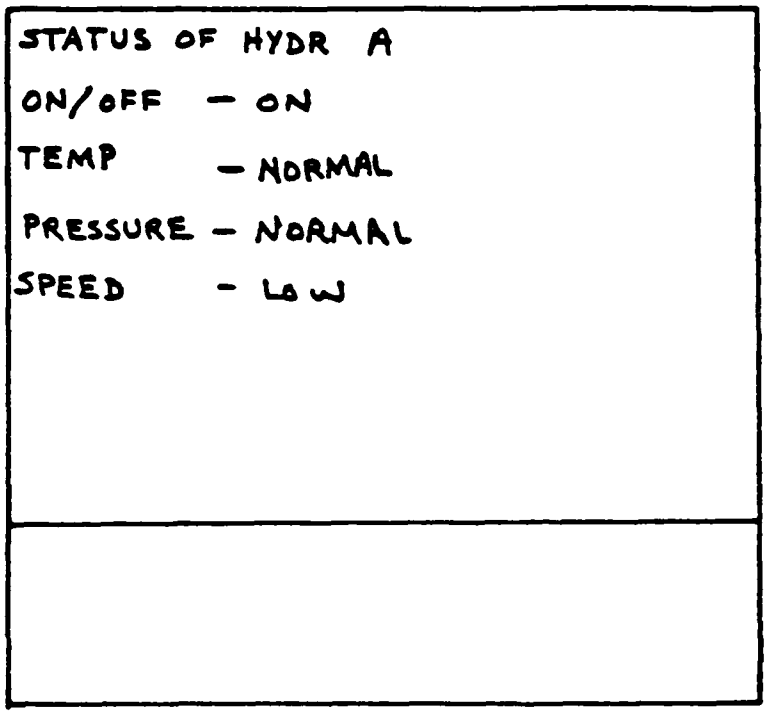

SELECT FUNCTION/SYSTEM
HYDR SYSTEM
A
COMM SYSTEM
B
FAULT
C
SELF TEST
D



HYDR A STATUS 1	HYDR B STATUS 2	HYDR C STATUS 3	TOP LEVEL 4

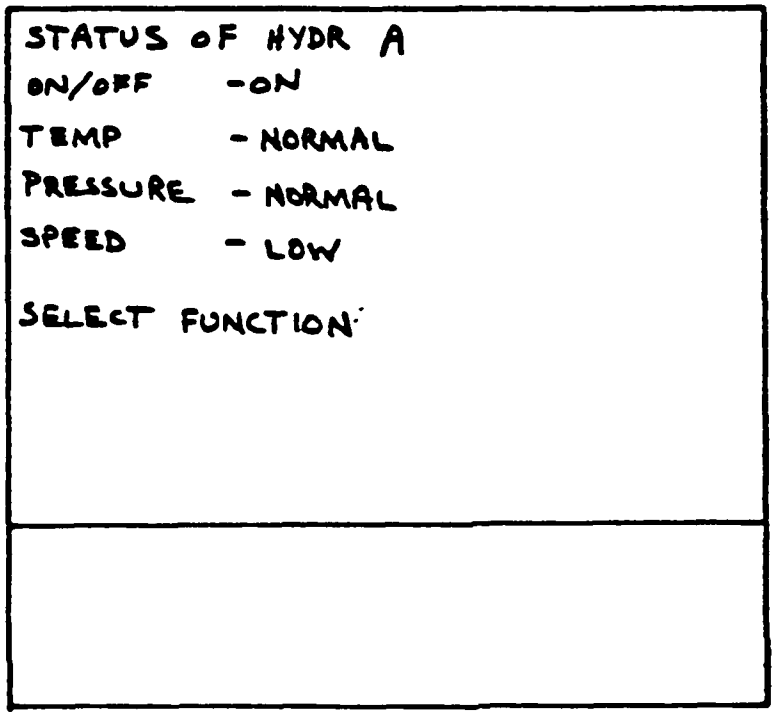


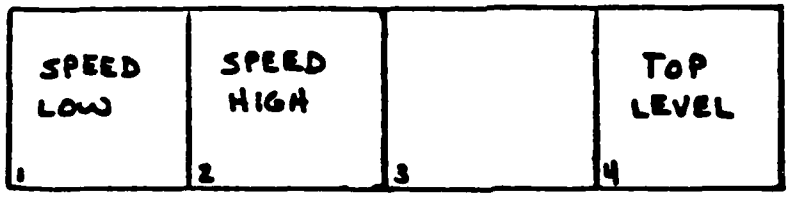
SPEED CONTROL 1	ON - OFF CONTROL 2	 3	TOP LEVEL 4

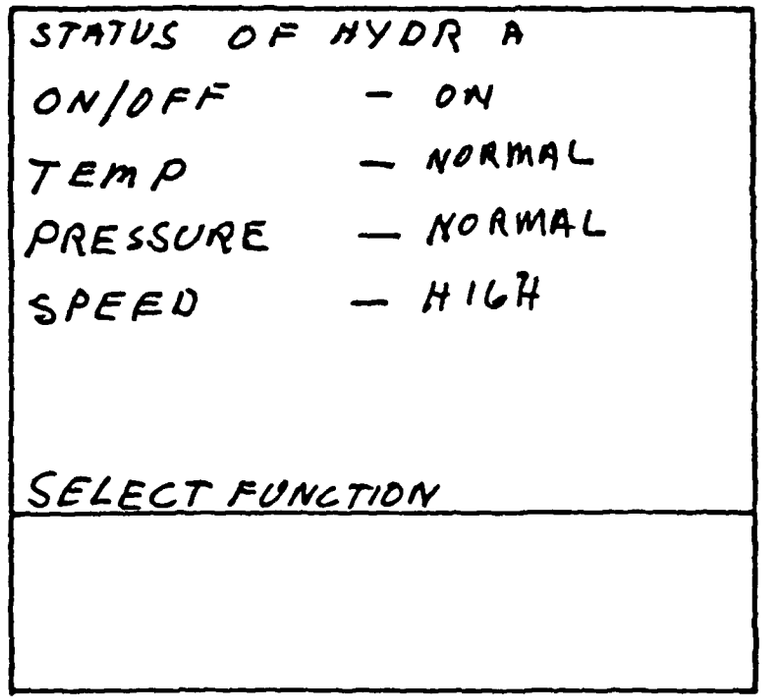


NOTE: NO DISPLAY change From 1A1, 1A2, 1A3.

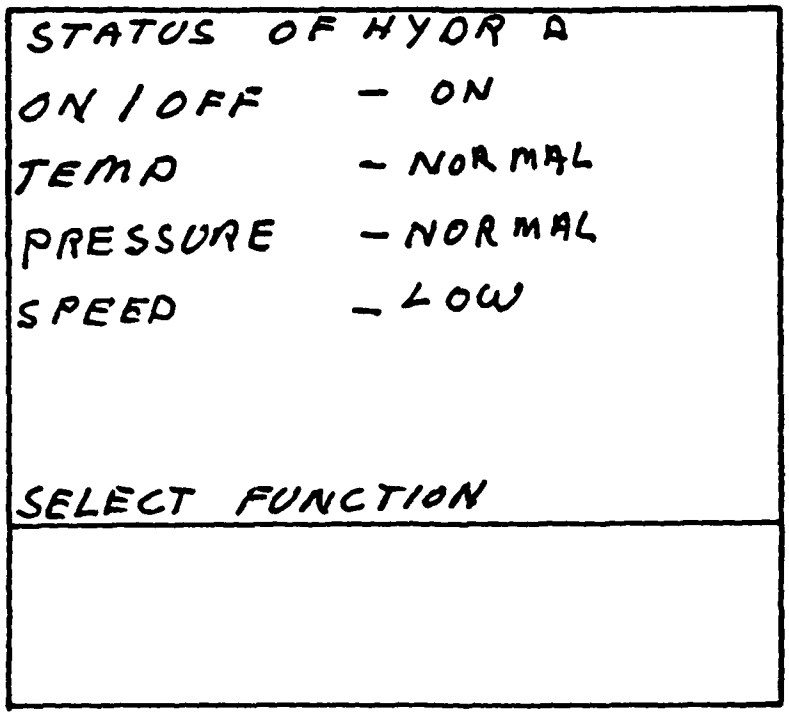
SPEED LOW 1	SPEED HIGH 2	 3	TOP LEVEL 4


STATUS OF HYDR A
ON/OFF -ON
TEMP - NORMAL
PRESSURE - NORMAL
SPEED - LOW
SELECT FUNCTION

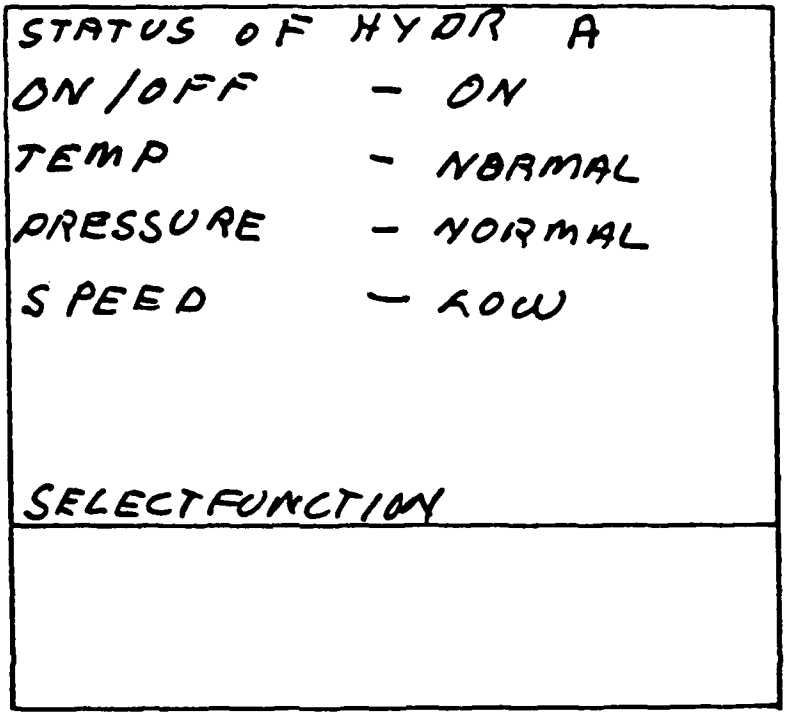

SPEED LOW
1
SPEED HIGH
2
3
TOP LEVEL
4



SPEED LOW	SPEED HIGH		TOP LEVEL
1	2	3	4



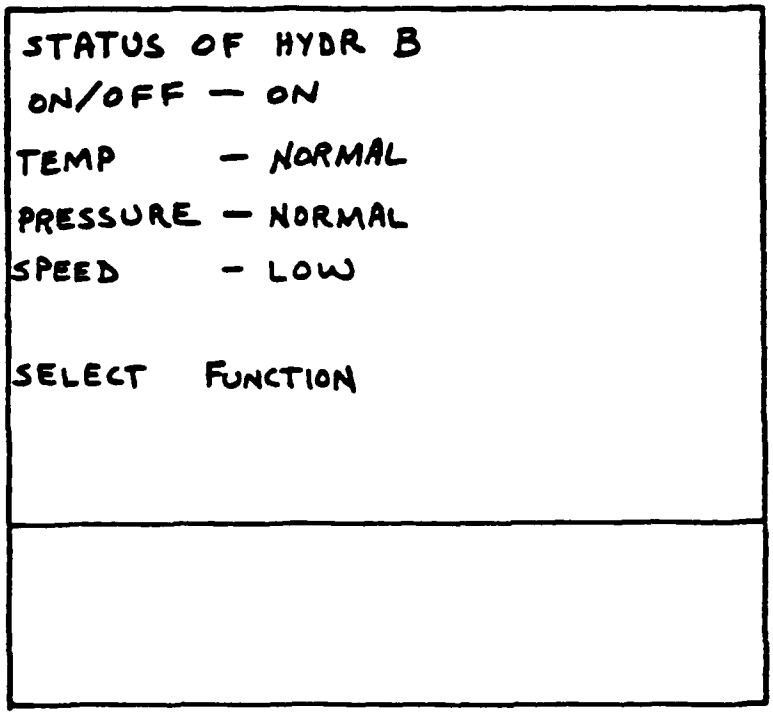
HYDR ON 1	HYDR OFF 2	 3	TOP LEVEL 4



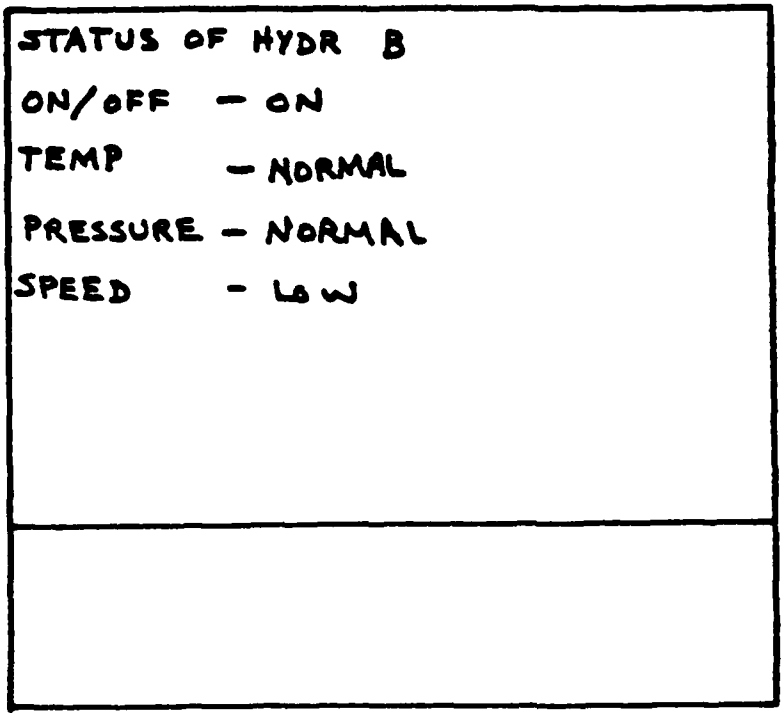
HYDR ON	HYDR OFF		TOP LEVEL
1	2	3	4

STATUS OF HYDR A
ON/OFF - OFF
TEMP - NORMAL
PRESSURE - OFF
SPEED - OFF
SELECT FUNCTION

#YDR ON 1	#YDR OFF 2	3	TOP LEVEL 4

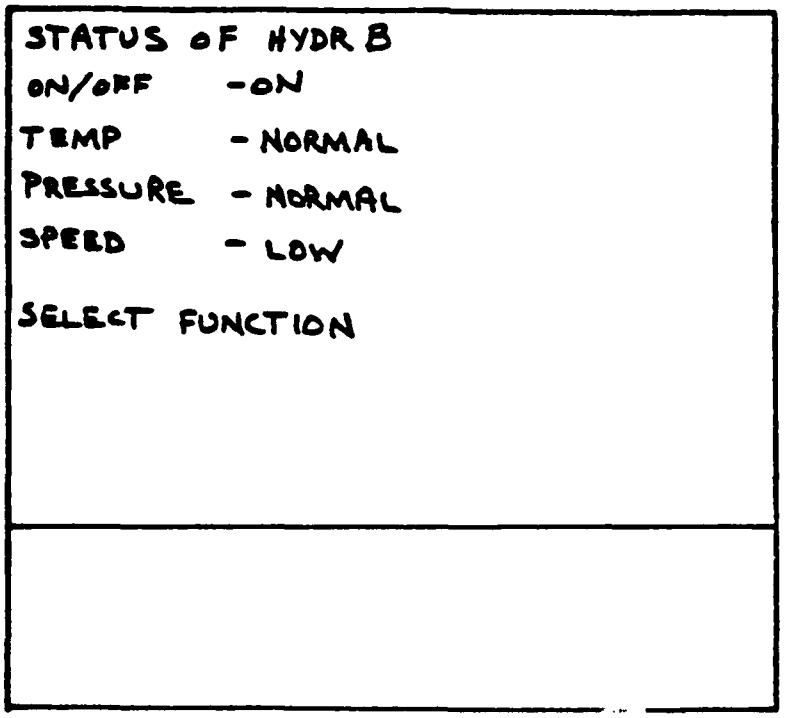


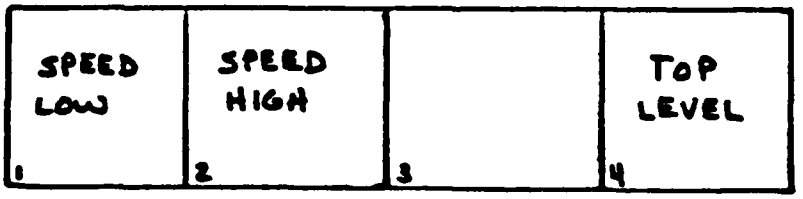
SPEED CONTROL 1	ON - OFF CONTROL 2	3	TOP LEVEL 4

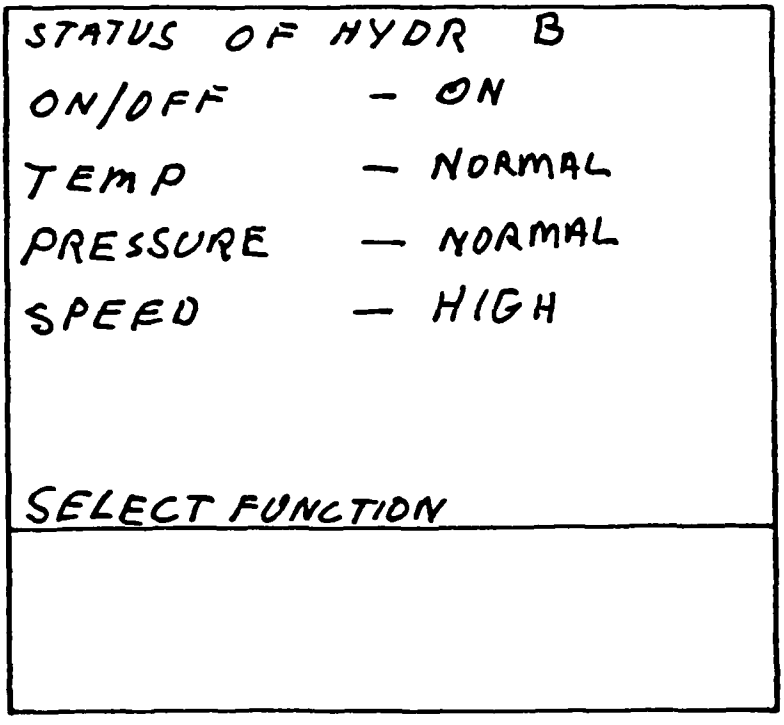


NOTE: NO DISPLAY change From 1A1, 1A2, 1A3.

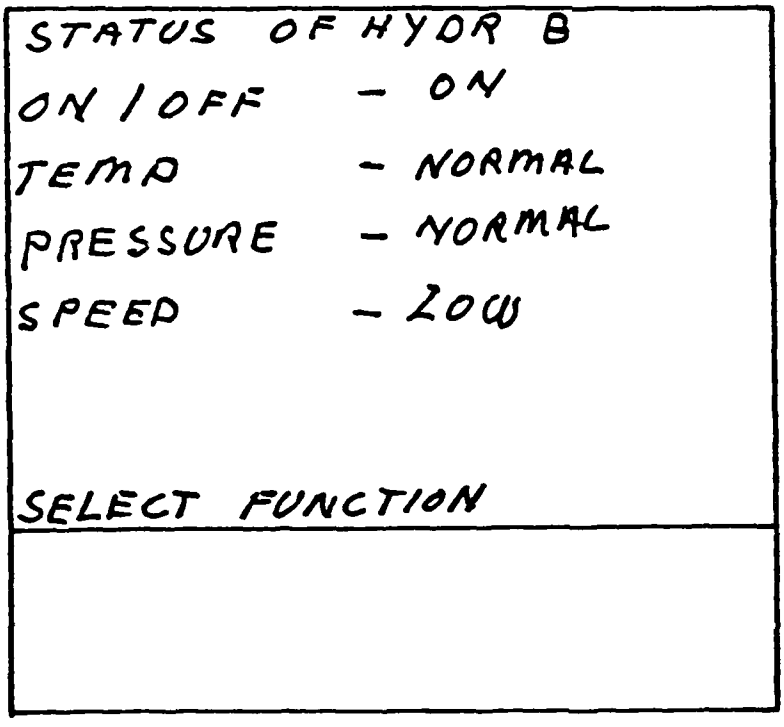
SPEED LOW 1	SPEED HIGH 2	 3	TOP LEVEL 4


STATUS OF HYDR B
ON/OFF - ON
TEMP - NORMAL
PRESSURE - NORMAL
SPEED - LOW
SELECT FUNCTION

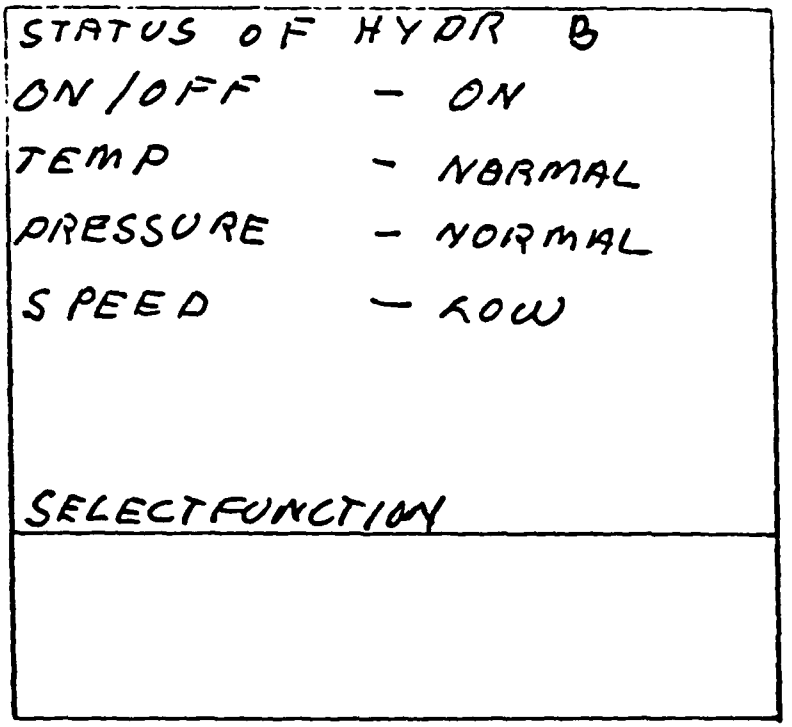

SPEED LOW
1
SPEED HIGH
2
3
TOP LEVEL
4



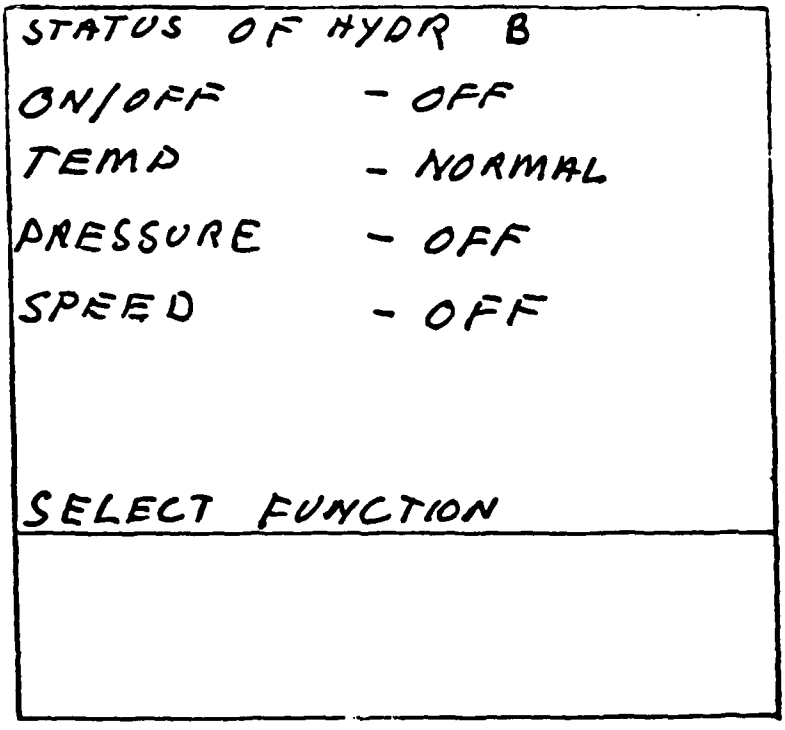
SPEED LOW	SPEED HIGH		TOP LEVEL
1	2	3	4



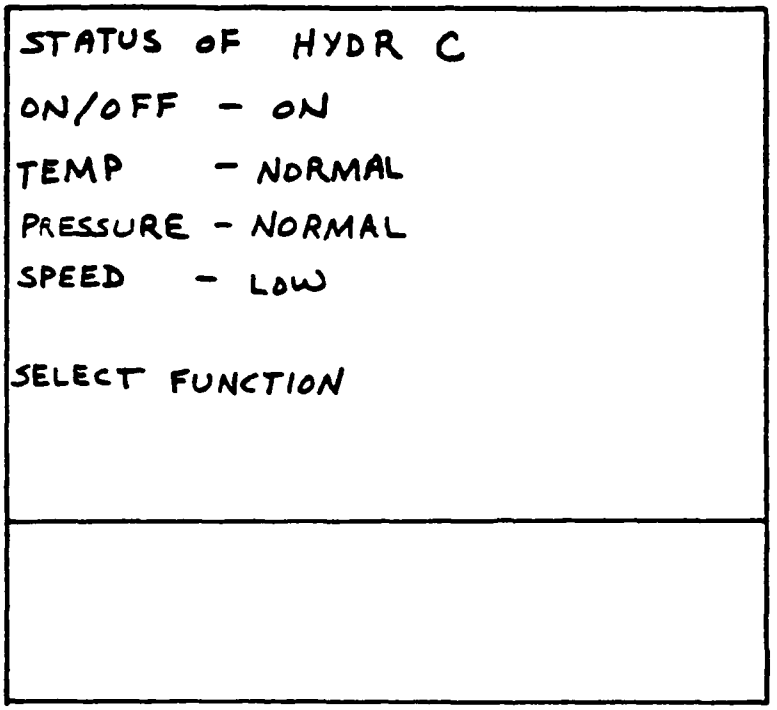
HYDR ON 1	HYDR OFF 2	3	TOP LEVEL 4



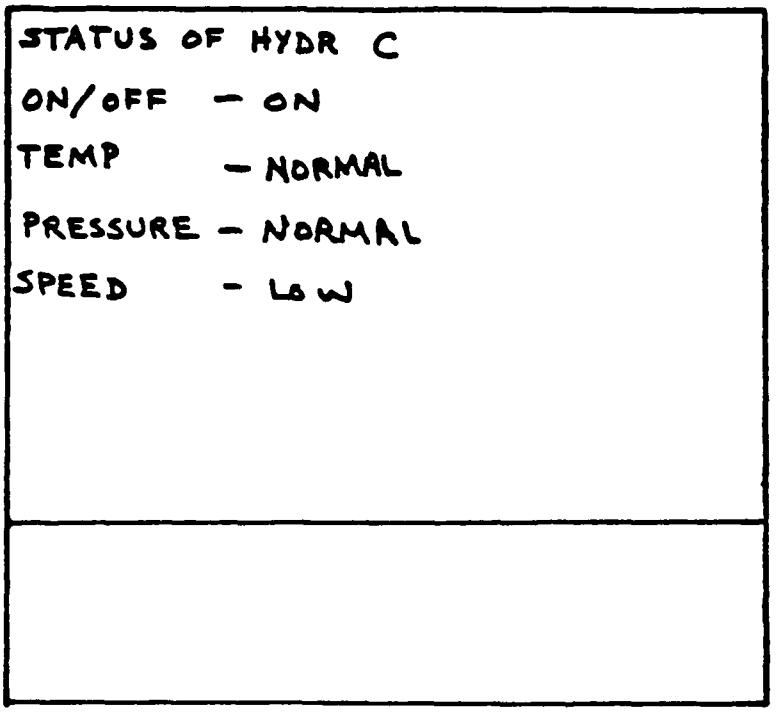
HYDR ON	HYDR OFF		TOP LEVEL
1	2	3	4



#YDR ON 1	#YDR OFF 2	3	TOP LEVEL 4

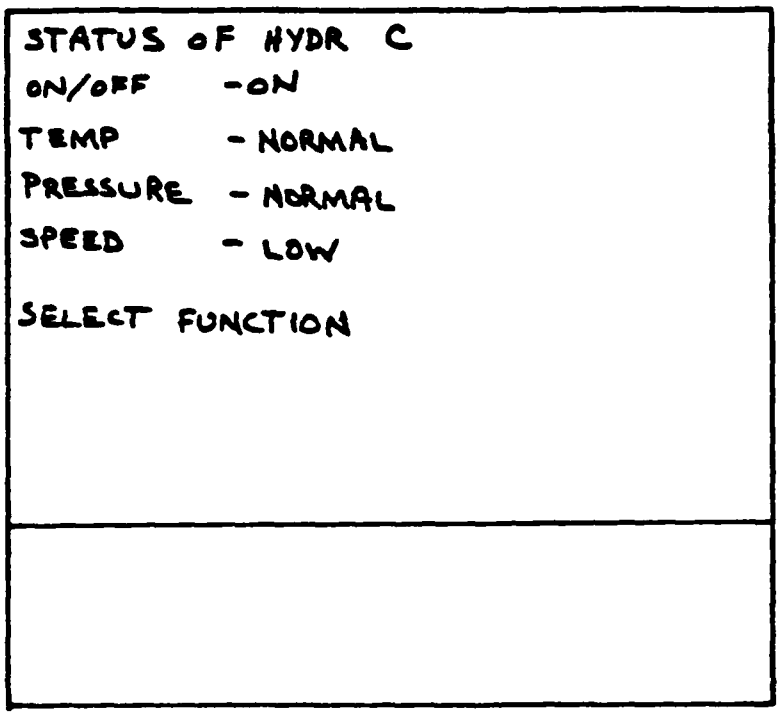


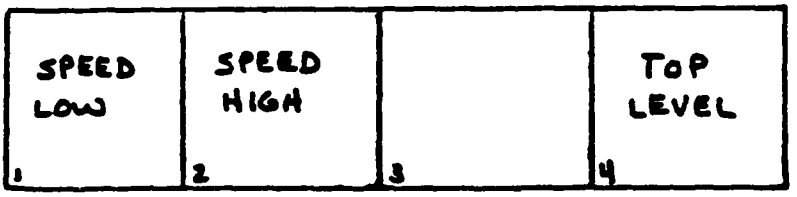
SPEED CONTROL	ON - OFF CONTROL		TOP LEVEL
1	2	3	4

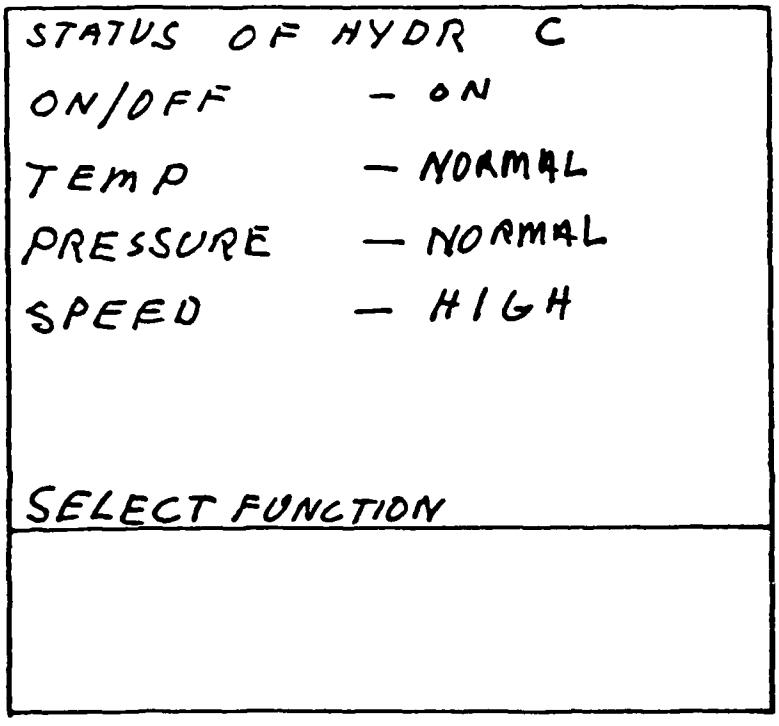


NOTE: NO DISPLAY change From 1A1, 1A2, 1A3

SPEED LOW	SPEED HIGH		TOP LEVEL
1	2	3	4


STATUS OF HYDR C
ON/OFF -ON
TEMP - NORMAL
PRESSURE - NORMAL
SPEED - LOW
SELECT FUNCTION

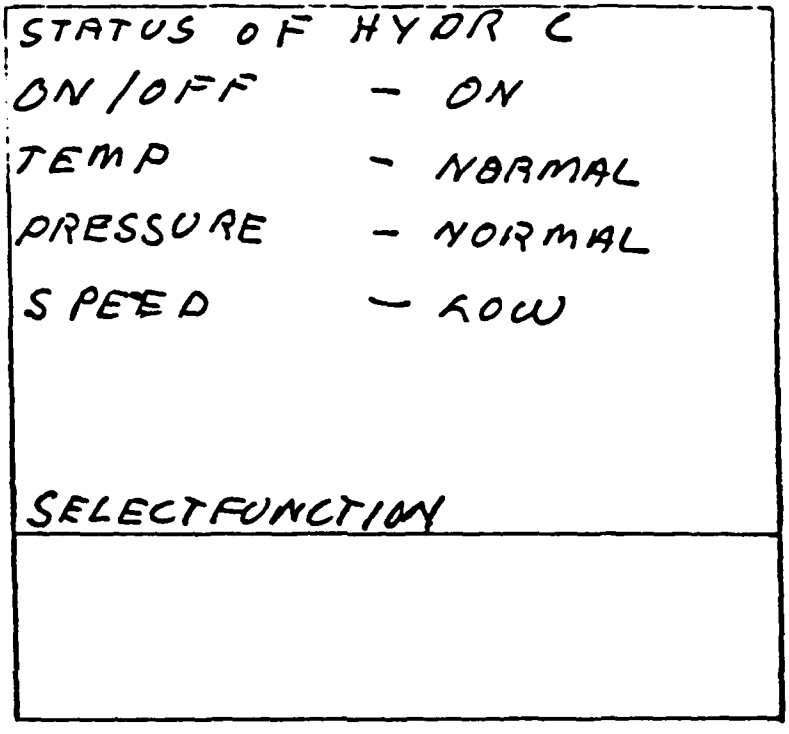

SPEED LOW
1
SPEED HIGH
2
3
TOP LEVEL
4



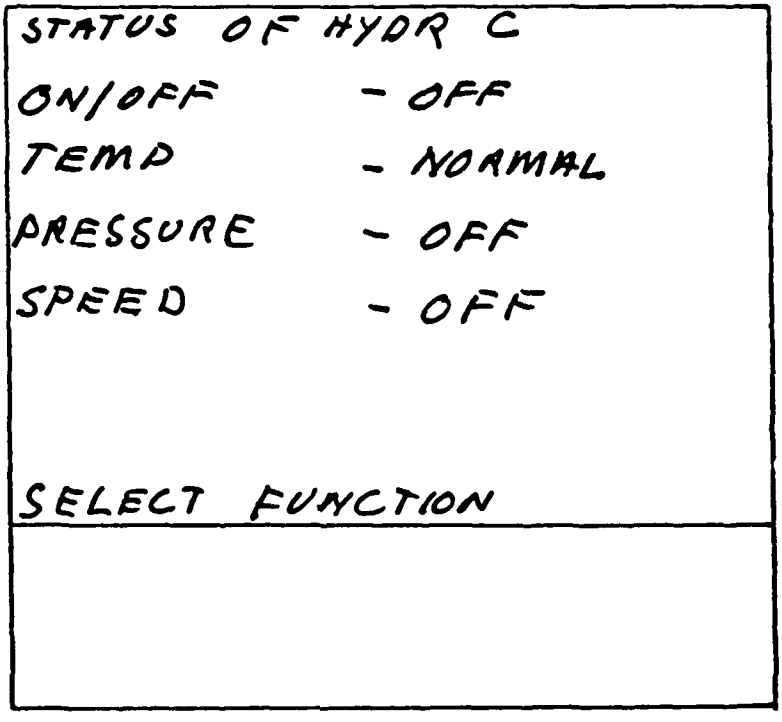
SPEED LOW	SPEED HIGH		TOP LEVEL
1	2	3	4

STATUS OF HYDR C
ON / OFF - ON
TEMP - NORMAL
PRESSURE - NORMAL
SPEED - LOW
SELECT FUNCTION

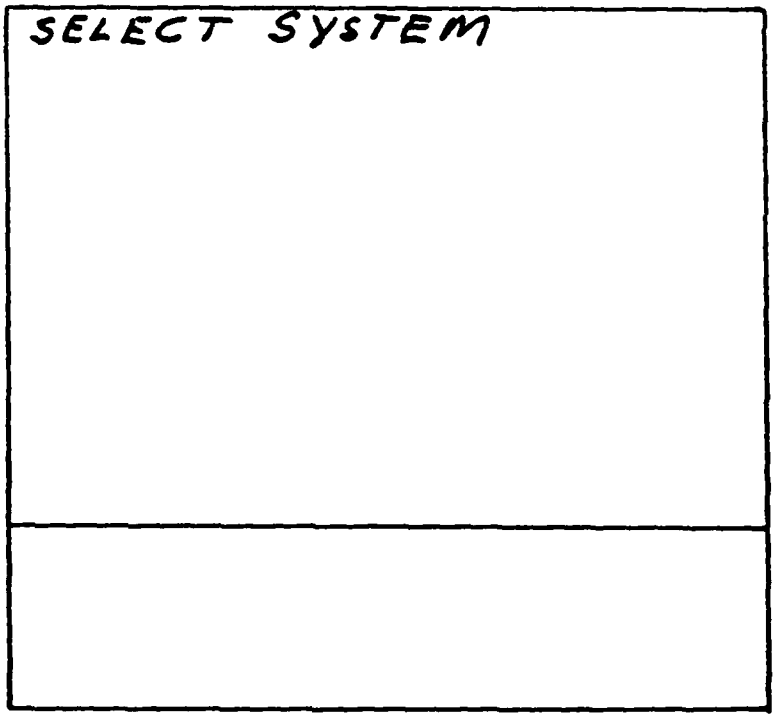
HYDR ON 1	HYDR OFF 2	3	TOP LEVEL 4



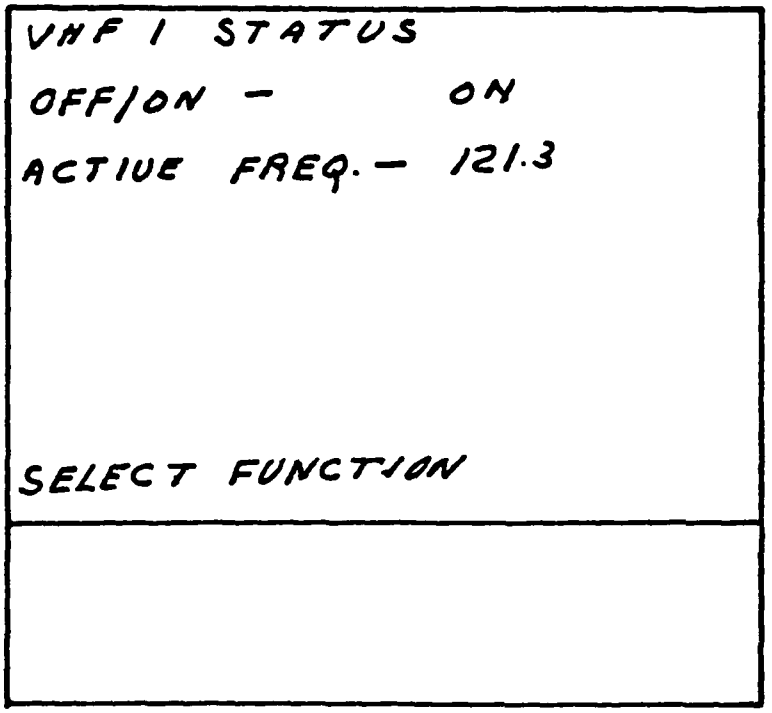
HYDR ON 1	HYDR OFF 2	 3	TOP LEVEL 4



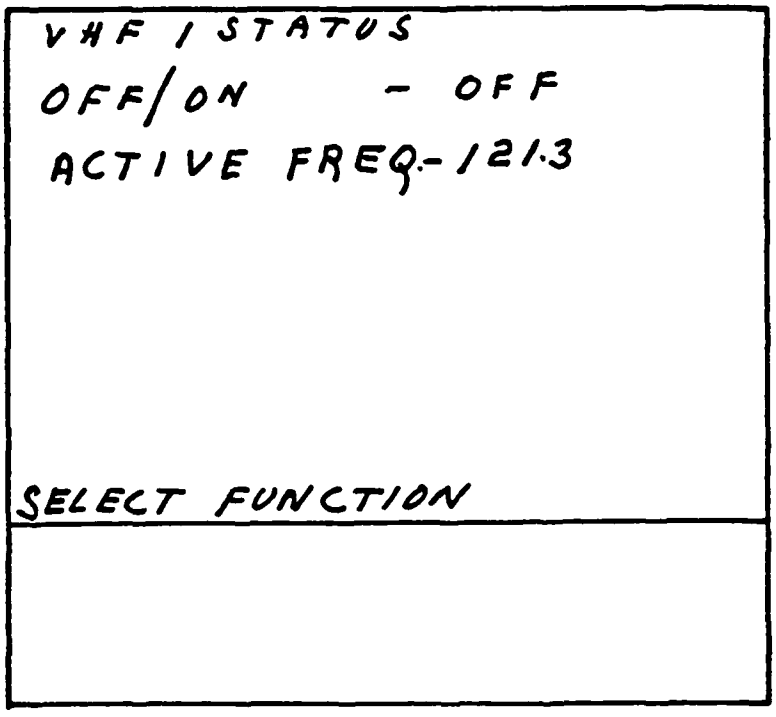
#YDR ON 1	# YDR OFF 2	3	TOP LEVEL 4



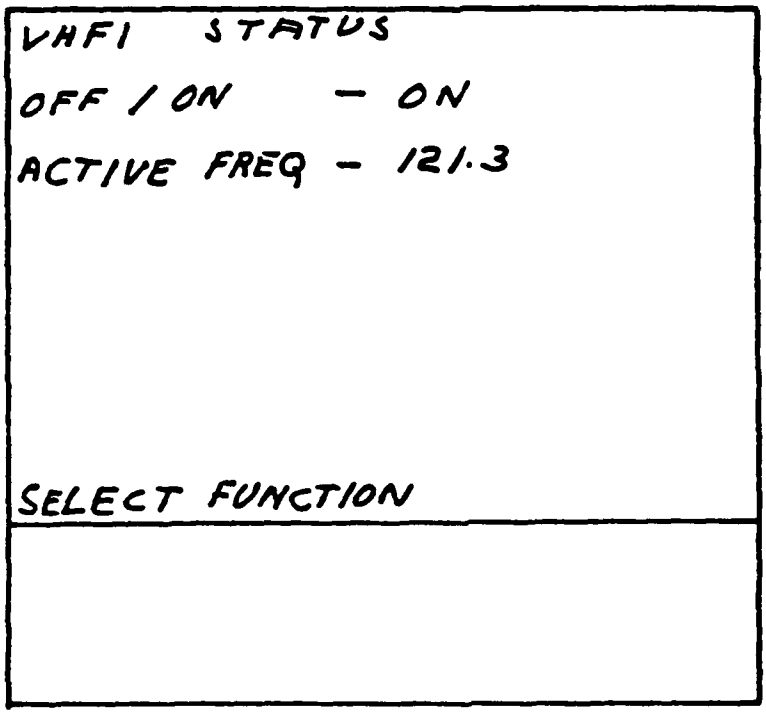
VHF 1	VHF 2	TACAN	TOP LEVEL
1	2	3	4



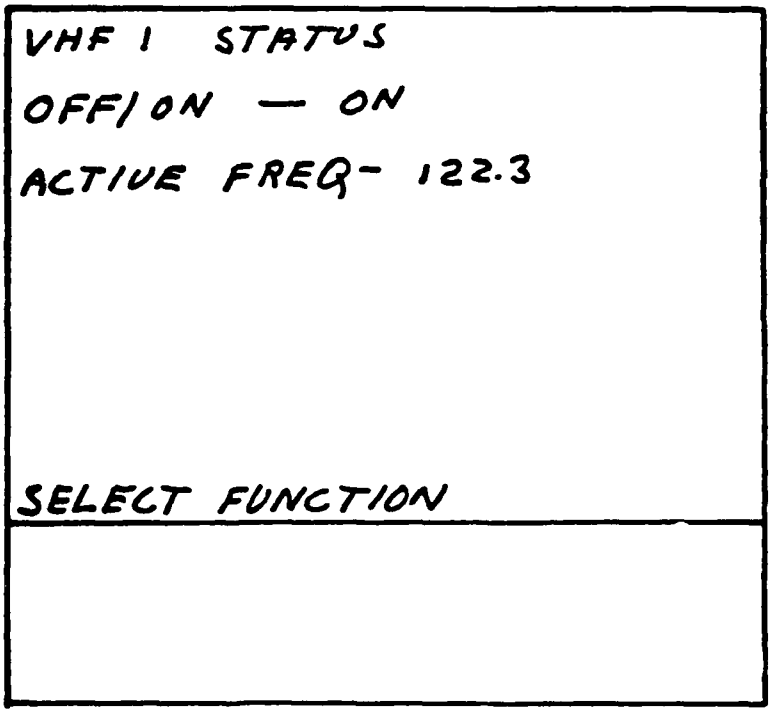
VHF 1	FREQ	FREQ	TOP
ON OFF	123.3	122.3	LEVEL
1	2	3	4



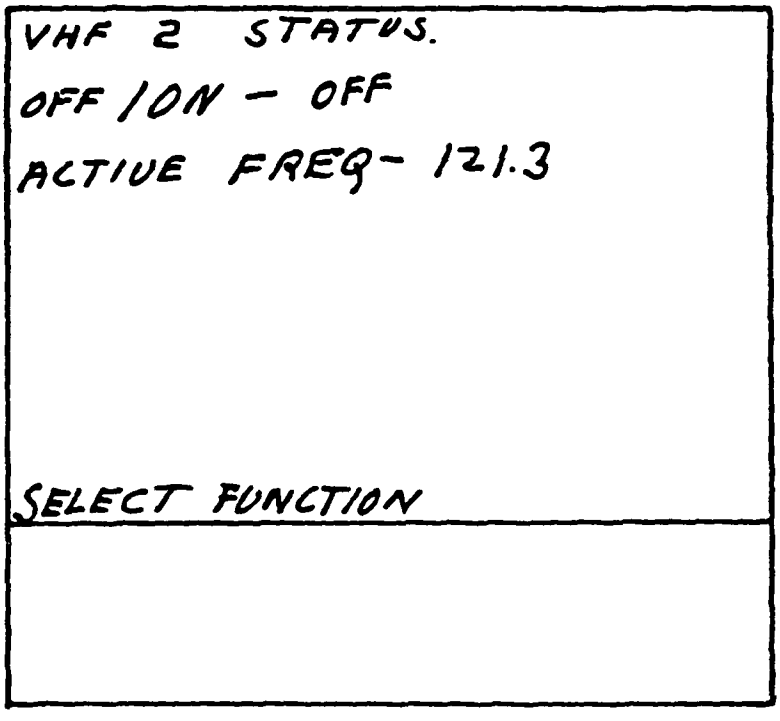
VHF 1	FREQ	FREQ	TOP
ON OFF	121.3	122.3	LEVEL
1	2	3	4



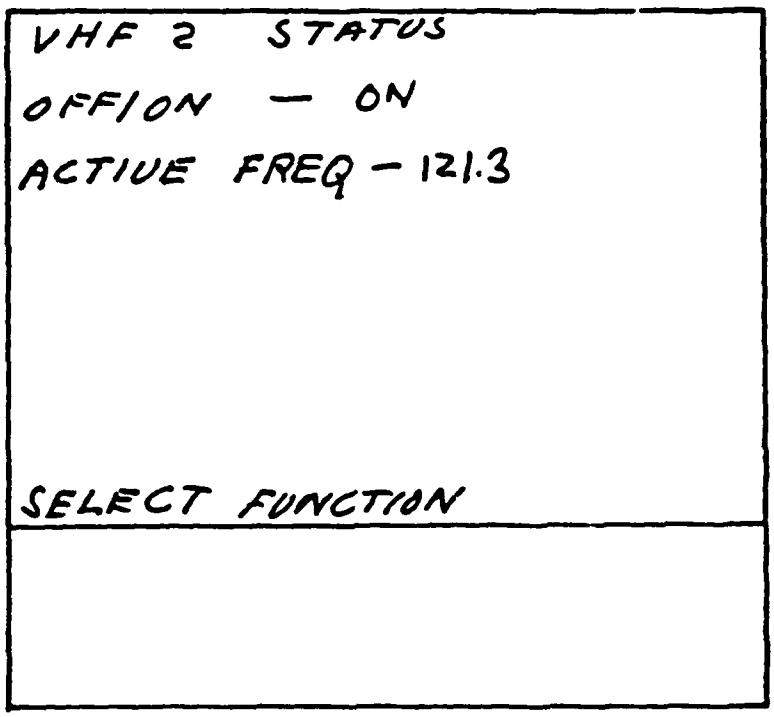
VHF1	FREQ	FREQ	TOP
ON OFF	121.3	122.3	LEVEL
1	2	3	4



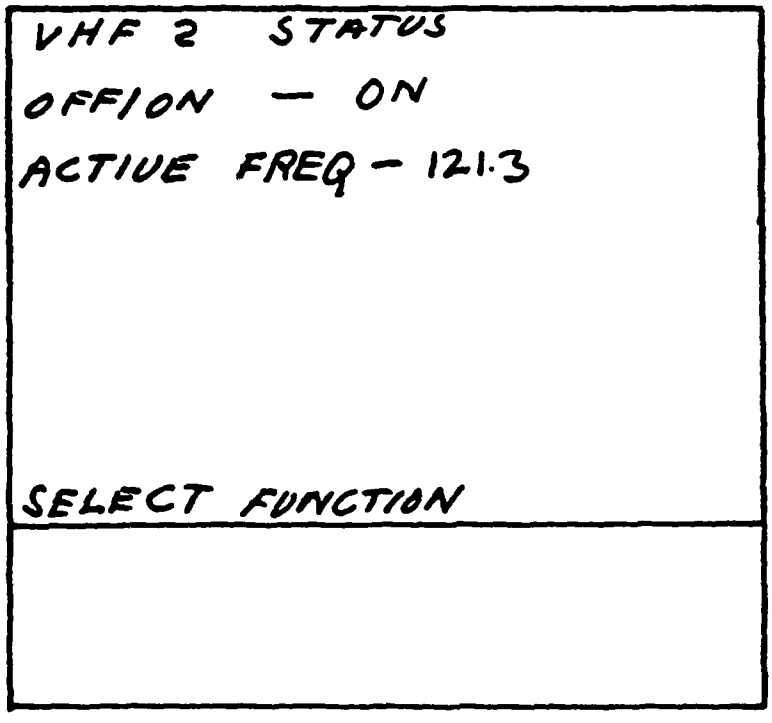
VHF 1 ON OFF 1	FREQ 121.3 2	FREQ 122.3 3	TOP LEVEL 4



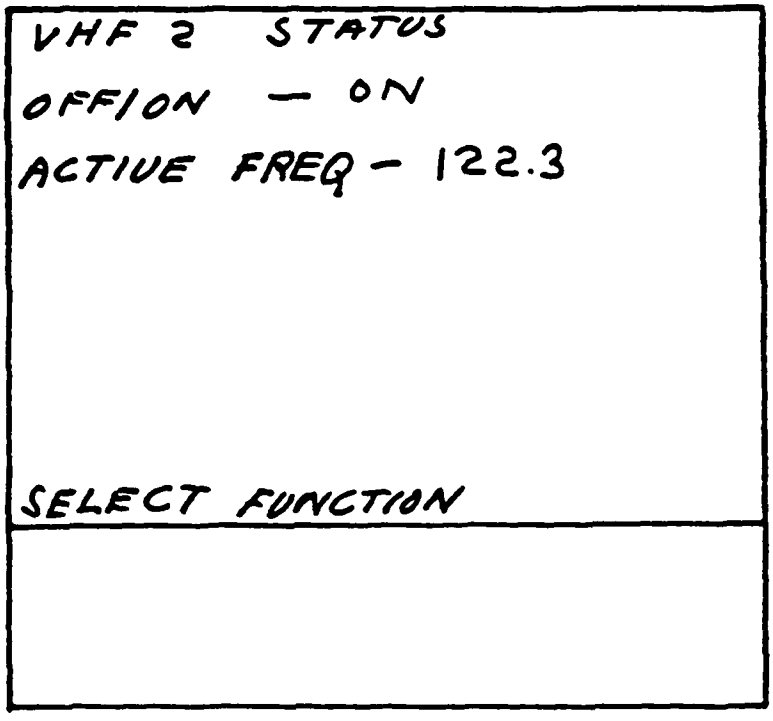
VHE 2	FREQ	FREQ	TOP
ON OFF	121.3	122.3	LEVEL
1	2	3	4



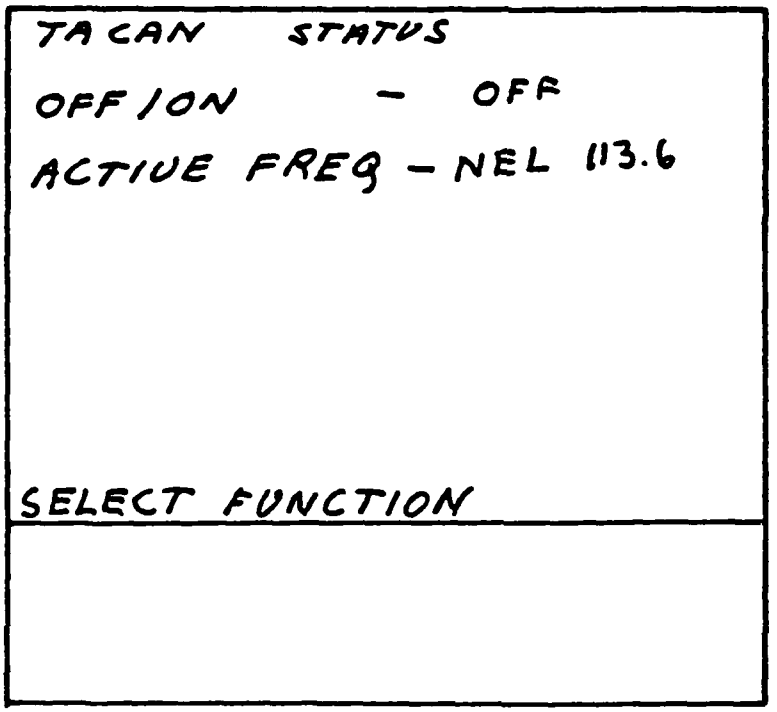
VHF 2	FREQ	FREQ	TOP
ON OFF	121.3	122.3	LEVEL
1	2	3	4



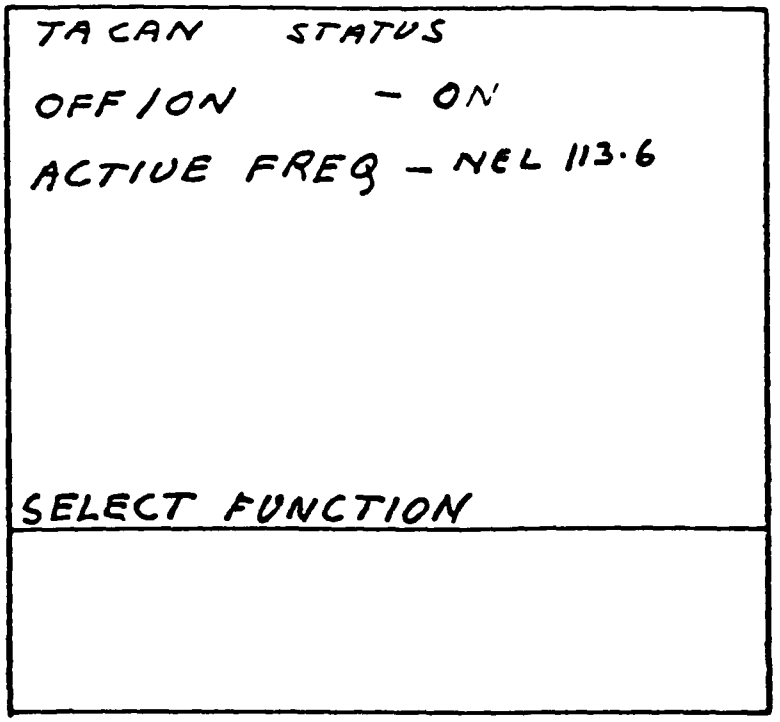
VHF 2	FREQ	FREQ	TOP
ON OFF	121.3	122.3	LEVEL
1	2	3	4



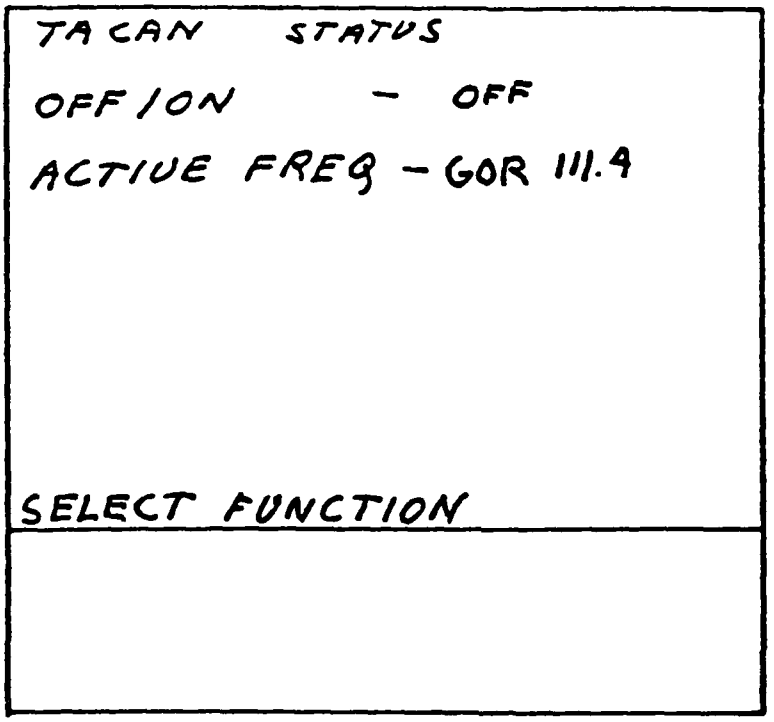
VHF 2 ON OFF	FREQ 121.3	FREQ 122.3	TOP LEVEL
1	2	3	4



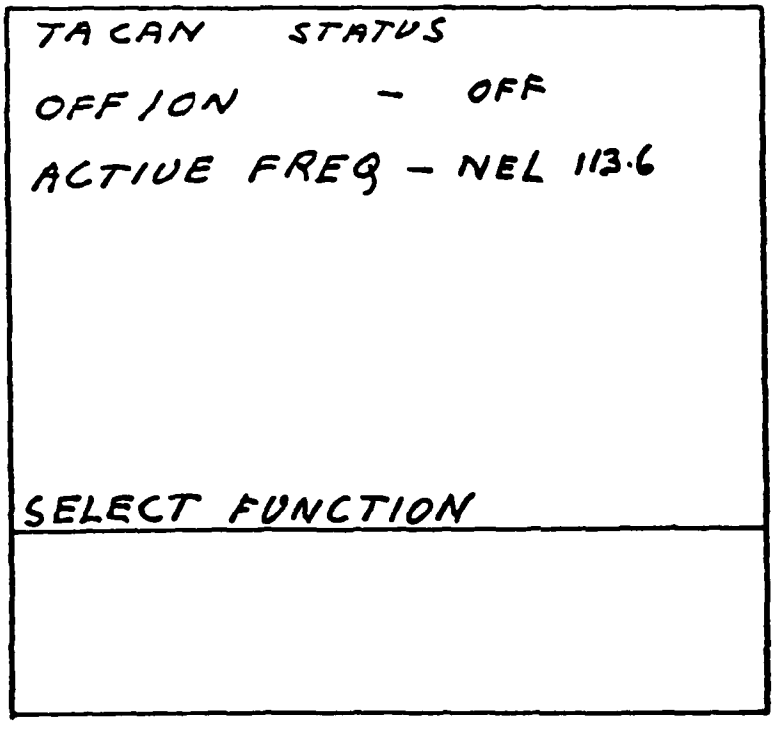
TACAN	(GOR)	(NEL)	TOP
OFF ON	111.4	113.6	LEVEL
1	2	3	4



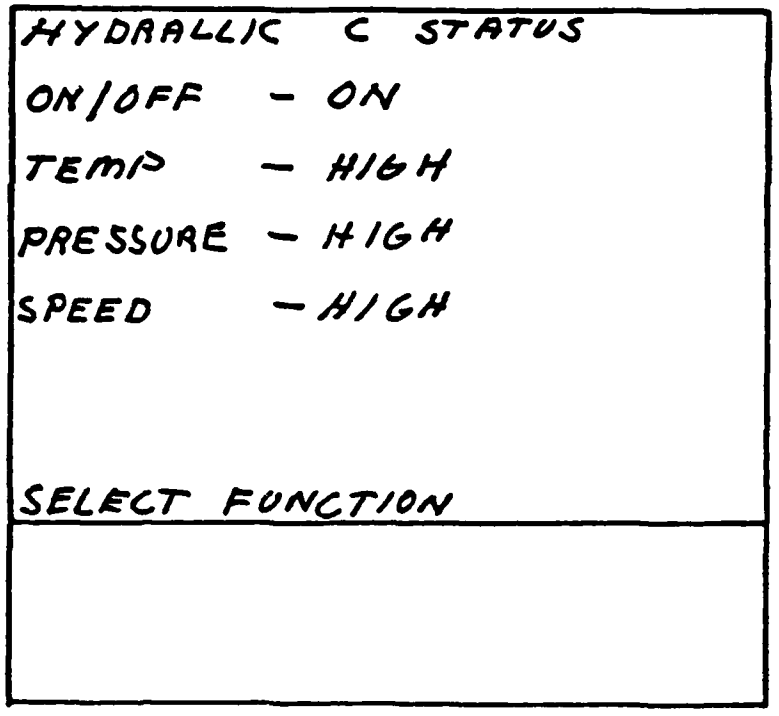
TACAN	(GOR)	(NEL)	TOP
OFF ON	111.4	113.6	LEVEL
1	2	3	4

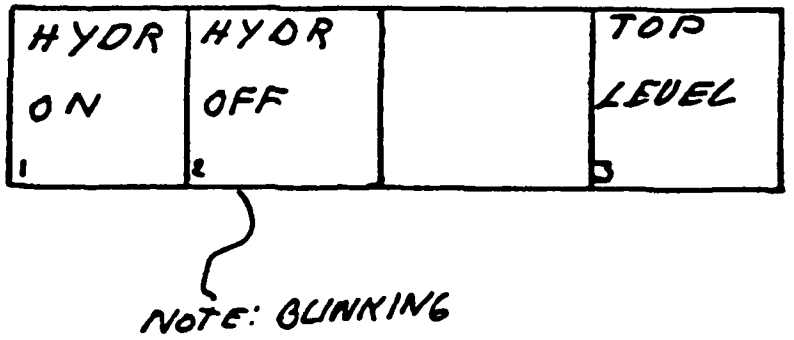


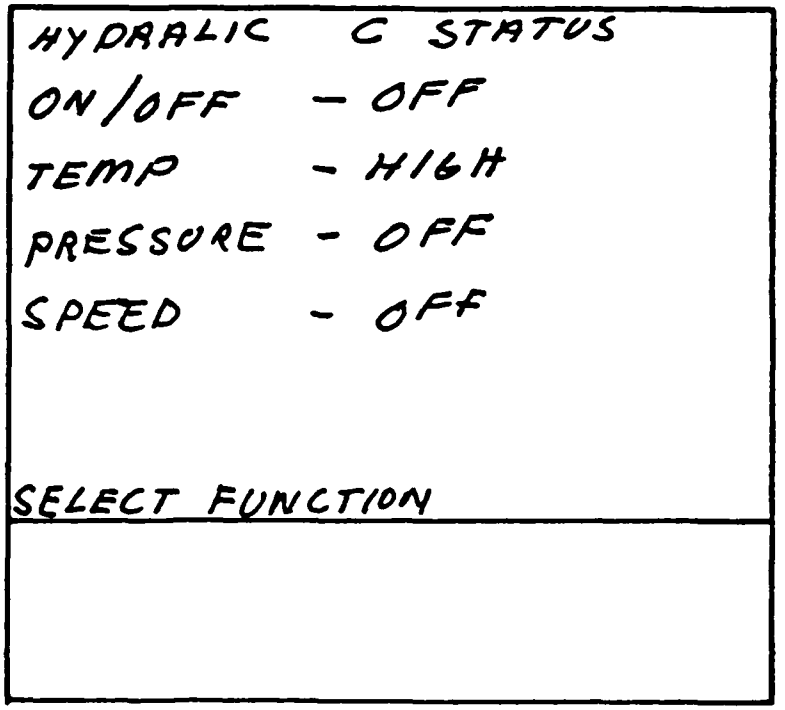
TACAN	(GOR)	(NEL)	TOP
OFF ON	111.4	113.6	LEVEL
1	2	3	4



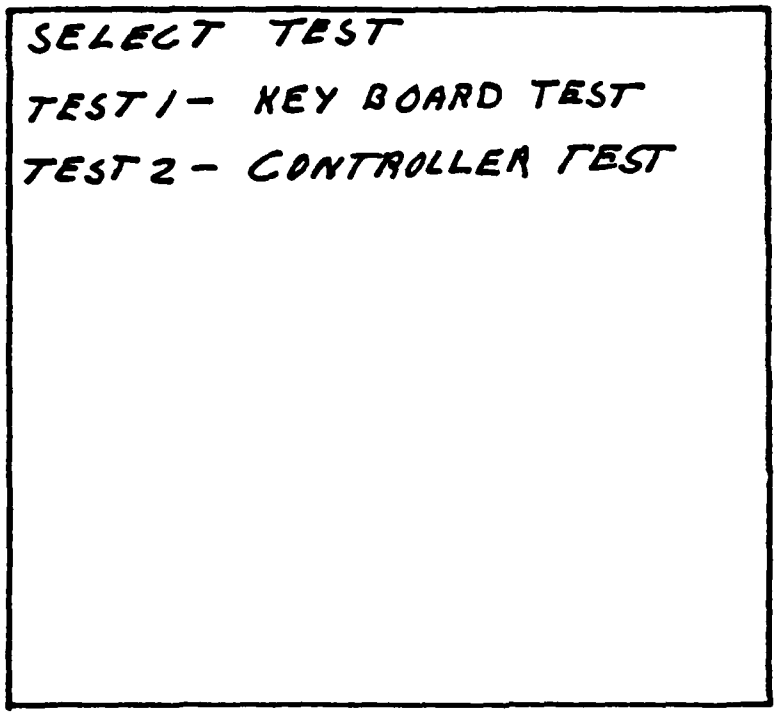
TACAN	(GOR)	(NEL)	TOP
OFF ON	111.4	113.6	LEVEL
1	2	3	4


HYDRALLIC C STATUS
ON/OFF - ON
TEMP - HIGH
PRESSURE - HIGH
SPEED - HIGH
SELECT FUNCTION

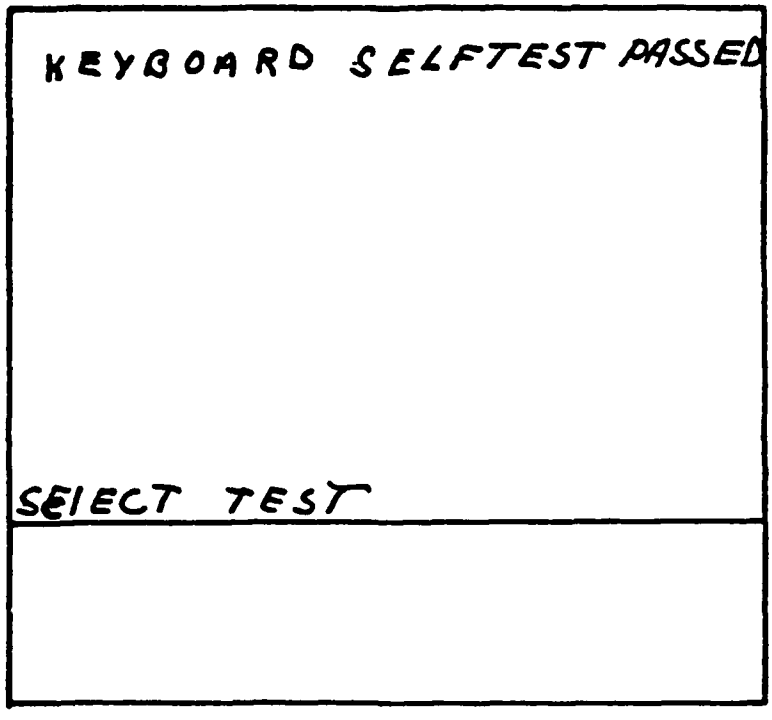

HYOR ON
1
HYDR OFF
2
TOP LEVEL
3
NOTE: BLINKING



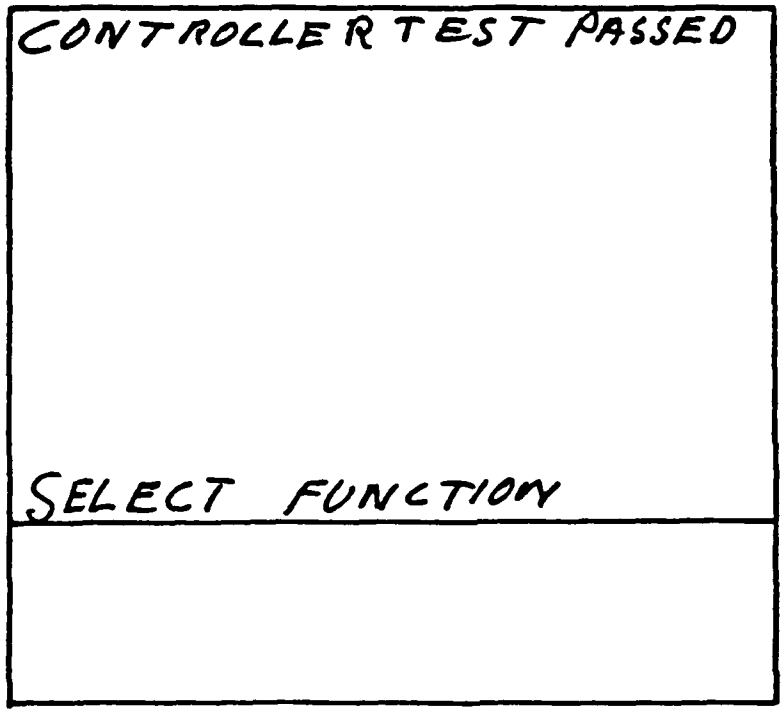
HYDR ON 1	HYDR OFF 2	 3	TOP LEVEL 4



TEST 1	TEST 2		TOP LEVEL
1	2	3	4



KEYB TEST 1	CONT TEST 2	3	TOP LEVEL 4



KEY B TEST 1	CONT TEST 2	3	TOA LEVEL 4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